Track and Hold Circuits

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Sec.10.5 (Allen & Holdberg); Sec 28.5 (Baker)
1. A track and hold circuit approximates a sample and hold circuit.
2. A non-inverting opamp is used in this implementation.
3. $v_C(t) = v_A(t)$ when the switch is on. In other words, it does not hold the sampled voltage in time. What gets sampled or held in the capacitor is the voltage before the switch is opened.
Non-Overlapping Clocks
1. $\Phi_S$ and $\Phi_H$ are non-overlapping clocks, i.e. $\Phi_S$ and $\Phi_H$ are not “on” at the same time.

2. $V_{in}$ is sampled when $\Phi_S = “1”$.

3. $V_{out}$ is only available when $\Phi_H = “1”$. 
$\Phi_S = "1"$ and $\Phi_H = "0"$

1. How is $V_{in}$ tracked or sampled when $\Phi_S = "1"$?
2. What does $V_{out}$ look like?
\[ \Phi_S = "0" \text{ and } \Phi_H = "1" \]

1. How does the sampled data become available at the output when \( \Phi_H = "1" \)?
2. What is \( V_{out} \)?
1. This SAH uses an inverting opamp.
2. What is the gain of this sample and hold circuit?
Φ_S = “1” and Φ_H = “0”

1. How is the input sampled?
2. What is V_{out}?
Φ_S = “0” and Φ_H = “1”

1. How is the output generated when Φ_H = “1”?
Complete Schematic

1. $V_{CM}$ are required when the supplies are $V_{DD}$ and GND.
Sample Waveforms

1. Left: $C_1 = 100 \text{ pF}$ and $C_2 = 100 \text{ pF}$.
2. Right: $C_1 = 200 \text{ pF}$ and $C_2 = 100 \text{ pF}$. 