Design of Row/Column Decoder

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Hodges, Jackson & Saleh, Sec.8.2
Let there be \( N \) stages.

1. Determine \( LEf = \left( \ldots LE_j LE_{j+1} LE_{j+2} \ldots \frac{C_{out}}{C_{in}} \right)^{\frac{1}{N}} \)
2. Calculate \( D \), the normalized path delay,

\[
D = \sum_j \frac{\tau_j}{\tau_{inv}} \left( \frac{C_{j, out}}{C_{j, in}} + \gamma_j \right) = \sum_j LE_j f_j + P_j
\]

3. Calculate the total path delay, \( \tau_{inv} D \).

4. Calculate \( C_j = \frac{LE_{j+1}}{LEf} C_{j+1} \).
   4.1 \( C_{j+1} \) is the output capacitance driven by the \( j + 1 \) stage.
   4.2 \( C_j \) is the input capacitance of the \( j + 1 \) stage.

5. Calculate \( W = \frac{C_j}{\alpha C_g} \), where \( \alpha \) is 3, 4, and 5 for, an inverter, a NAND2 and a NOR2, respectively. \( W \) is the width of a reference inverter.
Transistor-Level Schematic of Logic Gates

INV (left), NAND2 (middle), NOR2 (right)
**$LE_j$ and $P_j$ of Logic Gates**

<table>
<thead>
<tr>
<th></th>
<th>$LE_j$</th>
<th>$P_j$</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV</td>
<td>1</td>
<td>$\frac{1}{2}$</td>
</tr>
<tr>
<td>NAND2</td>
<td>$\frac{4}{3}$</td>
<td>1</td>
</tr>
<tr>
<td>NOR2</td>
<td>$\frac{5}{3}$</td>
<td>$\frac{3}{2}$</td>
</tr>
</tbody>
</table>

**Assumptions:**

1. 0.13 $\mu$m CMOS.
2. $t_{pd,fall} = t_{pd,rise}$. 
Two-Level Decoder for 256 Bit SRAM

1. $n = 4$ rows and $m = 4$ columns.
2. Each wordline is connected to $2^4$ cells.
3. Each precoder inverter is connected to $n$ decoder stages.
Estimate $C_{\text{wordline}}$

$C_g = 2 \ \mu F/\mu m; \ W/L = 0.5/0.1 \ \mu m/\mu m.$

1. How should $C_{\text{wordline}}$ be estimated? Ignore wire capacitance.
Logical Effort Analysis of the Row Decoder

1. How does the branching affect the optimal delay?
2. Show that $SE_{opt} = (LE_4 B_4 LE_3 B_3 LE_2 B_2 LE_1 B_1 \frac{C_{wordline}}{C_{in}})^{1/4}$. 
Optimum Stage Effort

Derivation:

1. \[ \frac{C_{\text{wordline}}}{C_{\text{in}1}} = \frac{C_{\text{wordline}}}{C_{\text{in}4}} \frac{C_{\text{in}4}}{C_{\text{in}3}} \frac{C_{\text{in}3}}{C_{\text{in}2}} \frac{C_{\text{in}2}}{C_{\text{in}1}} \]

2. \[ B_4 B_3 B_2 B_1 \frac{C_{\text{wordline}}}{C_{\text{in}1}} = B_4 B_3 B_2 B_1 \frac{C_{\text{wordline}}}{C_{\text{in}4}} \frac{C_{\text{in}4}}{C_{\text{in}3}} \frac{C_{\text{in}3}}{C_{\text{in}2}} \frac{C_{\text{in}2}}{C_{\text{in}1}} \]

3. \[ LE_4 LE_3 LE_2 LE_1 B_4 B_3 B_2 B_1 \frac{C_{\text{wordline}}}{C_{\text{in}1}} = LE_4 LE_3 LE_2 LE_1 B_4 B_3 B_2 B_1 \frac{C_{\text{wordline}}}{C_{\text{in}4}} \frac{C_{\text{in}4}}{C_{\text{in}3}} \frac{C_{\text{in}3}}{C_{\text{in}2}} \frac{C_{\text{in}2}}{C_{\text{in}1}} \]

4. \[ LE_j B_j \frac{C_{j+1,\text{in}}}{C_{j,\text{in}}} = LE_{j+1} B_{j+1} \frac{C_{j+2,\text{in}}}{C_{j+1,\text{in}}} \]

\[ SE_{opt} = \left( LE_4 B_4 LE_3 B_3 LE_2 B_2 LE_1 B_1 \frac{C_{\text{wordline}}}{C_{\text{in}}} \right)^{1/4}. \]
Logical Effort Analysis of the Row Decoder

$C_{\text{wordline}} = 32 \text{ fF, } C_{\text{in}} = 2 \text{ fF, and } \tau_{\text{inv}} = 7.5 \text{ ps. Assume 0.13 } \mu\text{m CMOS process.}$

1. Determine the normalized path delay.
2. Determine $f_j$ and $W_N$ of each stage.