DIGITAL INTEGRATORS

SUMMARY

This project describes techniques for digital integration. The object of the project is to design digital integrators and to interconnect two integrators to solve a second-order differential equation.

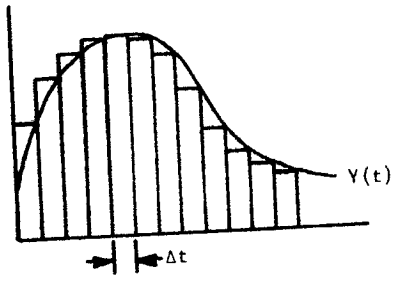

FIGURE E1-1 Digital integration.

DIGITAL INTEGRATION

As shown in Figure E1-1, an integral $\int Y(t)dt$ may be approximated by a sum of rectangle areas, $\Sigma Y(t)\Delta t$. The width of each rectangle is the iteration period, Δt, and the height of each rectangle is the value of $Y(t)$ where t is a multiple of Δt.

The iteration period Δt is the smallest quantum of time and hence it is represented as one unit digitally. Thus the area of each rectangle is numerically equal to its height. Keeping this in mind we can now describe a digital integrator. As shown in Figure E1-2, the device has two registers Y and I that contain signed quantities. The Y register holds the current value of the function $Y(t)$, and the I register accumulates the integral. During each iteration period, two operations take place.

1) The Y register is updated to hold the new value of the function $Y(t)$.

2) The new value of the Y register is added to the I register to form the current value of the integral.

Notice that the I register has twice as many bits as the Y register. Since the integral accumulates quickly when Y is large, I must be large enough to prevent overflow. The most significant n bits of I contain the usable integral with n bits of significance. This is somewhat akin to the $2n$-bit product of two n-bit numbers, in which the precision of the product is really only n bits, not $2n$ bits. The reason for choosing exactly $2n$ bits for I will become apparent later.

Practical digital integrators use an incremental representation to increase speed and simplify interconnections. Hence, instead of specifying a completely new value of Y in step (1) at each iteration period, only a ΔY increment of +1, -1, or 0 is specified. That is, the value of Y changes by at most +1 or -1 at each step. The Y register can then be a counter that at each iteration period either counts up, counts down or remains the same.

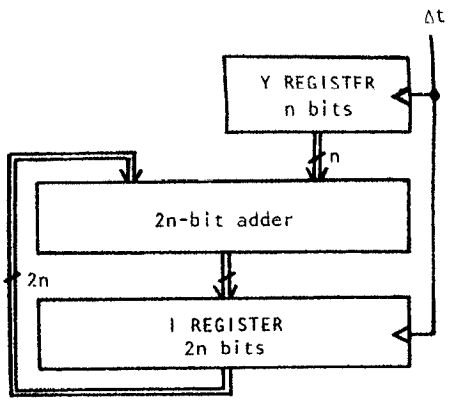

FIGURE E1-2 Digital integrator.

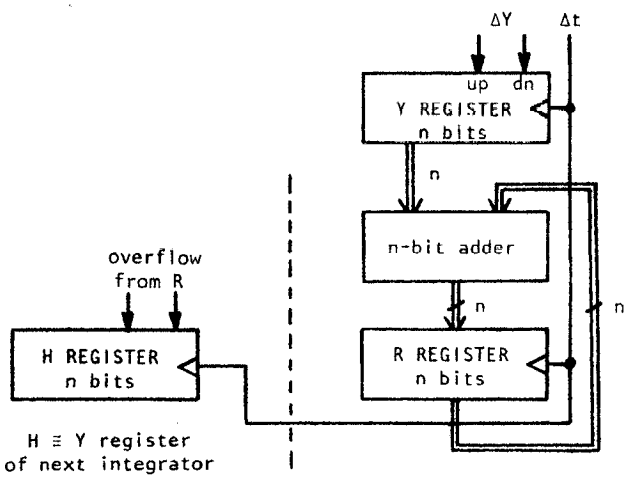

FIGURE E1-3 Incremental digital integrator.

We see that the input of a digital integrator is in an incremental form. For integrators to be interconnected to solve differential equations, the outputs must also have an incremental form. Consider the integrator of Figure E1-2 as re-drawn in Figure E1-3. The Y register has n bits and the I register is divided into an n-bit low order part R and an n-bit high order part H that contains the most significant bits and sign of the accumulated integral. Each time the Y register is added to R, the high order part can change by at most +1 or -1. Hence the overflow from the R register is the incremental output of the integrator. It indicates how much the accumulated integral changes at each step. Instead of providing an H register in each integrator, the incremental output is accumulated in the Y register of a succeeding integrator when integrators are interconnected to solve equations.

In this project you will build digital integrators that operate as described above. A single digital integrator consists of the circuitry in the right half of Figure E1-3 - an n-bit up/down counter, n-bit adder, and n-bit register - plus a small amount of combinational circuitry to generate the incremental output.

The number in the Y register will be assumed to be a two's-complement number. The incremental output that should be produced depends on the sign of Y and the carry out of the n-bit adder, as summarized in the following table:

Sign of Y	Output Carry	Incremental Output
+	0	0
+	1	+1
-	0	-1
-	1	0

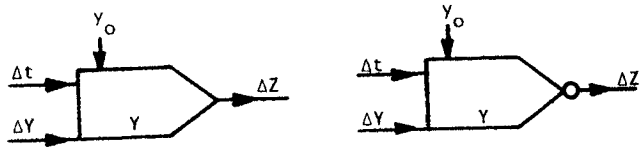

FIGURE E1-4 Integrator symbols.

That this table describes the correct behavior should be verified by considering the performance of the integrator of Figure E1-2 and extending the sign bit of Y to make it a two's-complement number with $2n$ bits.

The symbol for the digital integrator is shown in Figure E1-4(a), where Δt is the time quantum, ΔY is the incremental Y input, ΔZ is the incremental output, Y is the accumulated input, and Y_0 is the initial value of Y. It is possible to perform a sign inversion by swapping the +1 and -1 incremental signals, and Figure E1-4(b) is the symbol for such an inverting integrator. The output of an integrator is the integral of its input; equivalently, the input is the derivative of the output.

ASSIGNMENT

I. Design and construct an 8-bit integrator. Use an 8-bit up/down counter, an 8-bit adder, and an 8-bit register as the basic components. You will also need a small amount of combinational circuitry for deriving the incremental output. If 74191s are used for the up/down counter, then the format of the incremental output can be directly compatible with the 74191 count inputs. That is, it can consist of two signals that may be connected directly to the enable and up/down inputs of the counter in the next integrator. You should provide a push button and eight toggle switches for initializing the Y register and clearing the R register, an input for the Δt clock, and eight lamps for the counter output (Y). To aid you in the rest of the project, wire up a clock controller such as described in Project B1 or use a pulse burst generator.

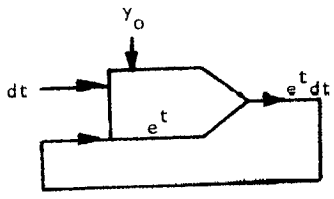

FIGURE E1-5 Exponential loop.

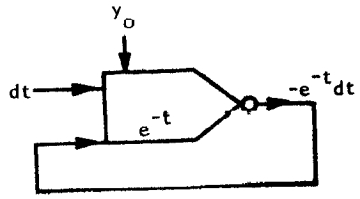

FIGURE E1-6 Negative exponential loop.

Using an initial condition of $y_0 = +32$, plot the output of the integrator from $t = 0$ to $t = 345$ in steps of 15. Plot the exact values of $32e^{N/256}$ given in Table E1-1 and compare.

III. Use an initial condition of $y_0 = -32$ to verify that your circuit works correctly for negative values of y.

IV. Hook up your integrator to invert and solve the equation $\frac{dy}{dt} + y = 0$, as shown in Figure E1-6. Use the initial condition $y_0 = +127$ and plot the integrator output for $t = 0$ to $t = 345$ in steps of 15. Plot the exact values of $127e^{-N/256}$ given in Table E1-1 and compare.

V. Build an integrator that replaces the adders and registers of Figure E1-3 with a 6-bit binary rate multiplier. (Leave the existing integrator intact.) Repeat Assignments II and IV with the BRM-based integrator and compare and comment on the results.

VI. Suppose you had to build a 12-bit integrator. What ICs would you need for a BRM-based integrator and for a register/adder integrator? What are the trade-offs?

VII. Dismantle the BRM-based integrator and build another register/adder integrator. Connect the two integrators in a sine-cosine loop to solve $\frac{d^2y}{dt^2} + y = 0$ as shown in Figure E1-7.

The first integrator has an initial condition of 0 and the second has initial condition y_0, the amplitude of the sine wave output. The accumulated integral in integrator 1 after N steps is approximately $y_0 \cdot \sin(N/256)$; and in integrator 2 the approximate function $y_0 \cdot \cos(N/256)$ is accumulated.

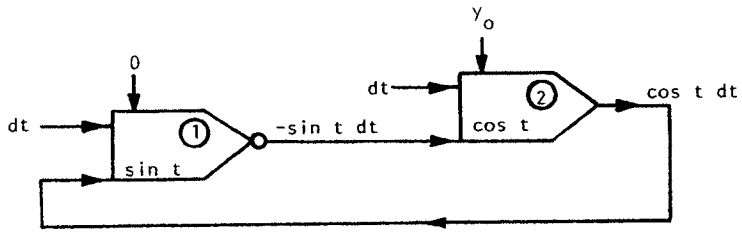

FIGURE E1-7 Sine-cosine loop.

TABLE E1-2 Sines and Cosines

N	100 sin(*N*/256)	100 cos(*N*/256)
0	0.0	100.0
30	11.7	99.3
60	23.2	97.2
90	34.4	93.9
120	45.2	89.2
150	55.3	83.3
180	64.7	76.3
210	73.1	68.2
240	80.6	59.2
270	87.0	49.3
300	92.1	38.8
330	96.1	27.8
360	98.6	16.4
390	99.9	4.7
420	99.8	-7.0
450	98.3	-18.6
480	95.4	-30.0
510	91.3	-40.9
540	85.8	-51.3
570	79.3	-61.0
600	71.6	-69.8
630	62.9	-77.7
660	53.4	-84.5
690	43.2	-90.8
720	32.3	-94.6
750	21.0	-97.8
780	9.5	-99.6
810	-2.2	-99.9

Plot the accumulated cosine integral for $t = 0$ to $t = 810$ in steps of 30, with an initial condition $y_0 = 100$. The exact values of $100 \cos(N/256)$ and $100 \sin(N/256)$ are given in Table E1-2. Plot the exact value of the cosine and compare.

VIII. Error analysis of the sine-cosine loop shows that the actual accumulated integrals in Assignment VII have the form

$$I_1 = k^N \sin N\alpha$$

$$I_2 = k^N \cos N\alpha$$

where $k = (1 + 1/M^2)^{\frac{1}{2}}$, $\alpha = \tan^{-1} 1/M$, and $M = 256$. Hence the accumulated integrals drift from the correct integrals in both amplitude and phase over periods of several cycles.

The solution of the equation $N/256 = 20$ is $N = 16085$, so that 16085 steps are needed for 10 cycles of the sine wave. With an initial condition of $y_0 = 100$, observe the drift for 10 cycles of the sine wave by making 10685 steps. The computed value of k^{16085} is 1.13, and hence the amplitude of the sine wave after 10 cycles should be about 113. The phase drift, on the other hand, is not observable after this few cycles.

IX. The integrator loop designed above is of the "simultaneous" variety, because all of the integrators change at the same time. A "sequential" scheme can also be used, in which one integrator changes before the other. Modify your sine-cosine loop to make it sequential by providing two clocks and updating one integrator with the first clock and the other with the second, as shown in Figure E1-8. Hence, the first integrator is updated, then the second, then the first, etc.

Error analysis of the sequential scheme indicates that all errors are either sinusoidal or bounded, so that this scheme does not exhibit the phase or amplitude drifts of the simultaneous scheme. Verify this by running the new sine-cosine loop for a long time.

X. Hook up an 8-bit DAC to the sine wave integral (invert the sign bit to get a proper signed display), and observe the DAC output on an oscilloscope. Neglecting DAC settling, what is the smallest Δt for which your system will work? What is the real-time frequency of the sine wave for this Δt?

Slow down the frequency of the system so that DAC settling is not a problem. Hook up an analog sine wave generator to the second scope channel and compare the two waveforms.

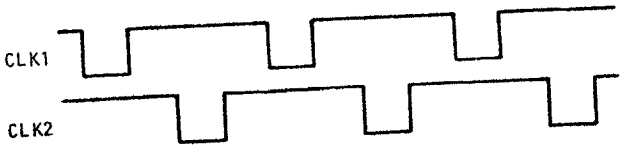

FIGURE E1-8 Two-phase clock.

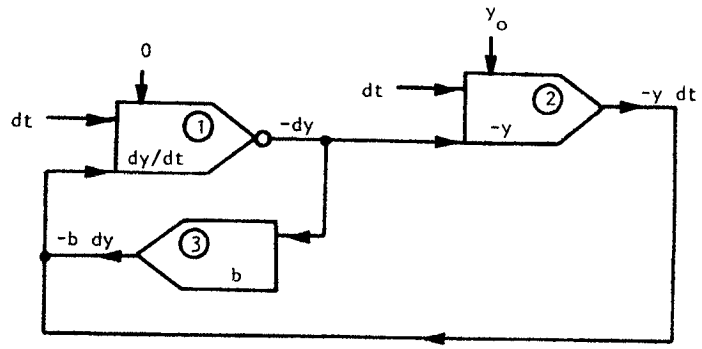

FIGURE E1-9 Damped sine-cosine loop.

XI. Modify your system to produce damped sine waves by solving the equation $\frac{d^2y}{dt^2} + b\frac{dy}{dt} + y = 0$, as shown schematically in Figure E1-9.

In Figure E1-9, integrator 3 performs multiplication by a constant. The Y register of integrator 3 is initially loaded with the constant b and does not change during the integration (the ΔY input is not used). Whenever +1 increments are produced by integrator 1, integrator 3's Y register is added its R register; when -1 increments are produced, -Y is added to R. The incremental output of integrator 3 is derived from the overflow of R in the usual manner.

Implement integrator 3 as a 4-bit integrator. Since the Y-register does not change, you may simply use 4 toggle switches or a wired connection to set the value of b.

The ΔY input of integrator 1 must respond to the outputs of both integrators 2 and 3. Therefore you will need circuitry to combine the two outputs. You may want to implement a two-phase system in which integrator 1 responds first to the output of integrator 2 and then to integrator 3. The overall system operation may be simultaneous or sequential.

Provide some circuitry for resetting the initial conditions automatically when the output amplitude becomes small. Then display the output on the oscilloscope. Observe the exponential decay and the frequency of the output for various values of b. What is the solution of the differential equation being emulated?