ECE 526

Verilog: Modeling, Simulation and Synthesis
ECE 526: Verilog HDL for Digital Integrated Circuit Design
Prerequisite: ECE 320/L. Corequisite: ECE 526L. This course covers use of Verilog Hardware Description Language for the design and development of digital integrated circuits, including mask-programmed ASICs and FPGAs. Hierarchical top down vs. bottom up design, synthesizable vs. non-synthesizable code, verification, hardware modeling, simulation system tasks, compiler directives and subroutines are all covered and illustrated with design examples. Lab exercises emphasize use of professional compilation and simulation tools for debugging and verification.
Instructor

- Dr. Ronald W. Mehler
- Jacaranda 3303
- (818) 677 2495
- Office Hours: Tuesday & Thursday, 2:00 – 3:00
Course Web Page

http://www.csun.edu/~rmehler/mehler_files/ece_526.htm
Prerequisite

ECE 320: Theory of Digital Systems
  Boolean algebra, combinational and sequential circuits, number systems, etc.

Advised:
  At least two 400-level computer engineering courses such as 420, 422 and 425.

Neither ECE526 nor any other 500-level course is a beginner’s course.
Books


Interesting Reading:


Lab Manual

- ECE 526 Verilog HDL Laboratory
- Purchase photocopy at CSUN Bookstore
- Updated for this semester
Lab Access

• To use the lab, you will need a user ID and password.
• If you are registered, you should have one of each.
• If you don’t know what yours are, see the web site
  – http://www.csun.edu/it/helpdesk/outages/accounts.html
COURSE POLICY

1. Homework and laboratory exercises will be assigned. They will be collected on due dates. Keep a copy of all solutions because homework solutions might not be returned. **No late homework** will be accepted.

2. Three exams will be given (two midterm exams and one final exam). Tentative dates of the midterm exams are Tuesday, October 6 and Tuesday, November 10.

3. Exam solution should be in **Blue Books**. (These can be bought at the bookstore.) **Absolutely** no other solution papers will be accepted. The Blue Books will be collected at the beginning of the semester and returned back on the exam day.

4. Exams are cumulative; study everything for every exam.

5. Absolutely **no make-ups** on exams. For emergency, you will be allowed to miss only one midterm exam with no penalty. The final exam **must** be taken to pass the course.
COURSE POLICY

6. The weights of the exams and exercises will be as follows:
   
   Exam #1 30%
   Exam #2 30%
   Final Exam 35%
   
   Total 95%

7. The remaining 5% will be given on homework as well as the general impression given by each student. Talking to neighbors or coming late to the class disturbs the class and give a bad impression. Please avoid doing that and participate in classroom discussions to guarantee a big portion of the 5%.

8. Your final grade will directly reflect the total number of points you will get. The following are the percentages for each grade:

   Grade A  90-100%  Grade C  68-75%
   Grade A-  85-90%  Grade C-  65-68%
   Grade B+  82-85%  Grade D+  60-65%
   Grade B   78-82%  Grade D   55-60%
   Grade B-  75-78%  Grade D-  50-55%
   Grade C+  72-75%  Grade F   Below 50%
Course Policy

• ECE 526 and ECE 526L are separate courses.
• Courses are co-requisites. It is required to take both concurrently.
• ECE 526L grade will be solely the average of all lab reports.
• Lab reports will have no bearing on ECE 526 grade.
Academic Dishonesty

• Claiming credit for someone else’s work is the ultimate sin in academia.
• Your instructor is as hard core as they come on this.
• Not only will cheating result in an F in the course, it may result in expulsion from the university.
• International students found guilty of academic dishonesty may be deported.
It’s NOT a Victimless Crime

• Giving diplomas to engineers who don’t know engineering quickly damages the reputation of the university.

• A cheater prevents those who come after from even getting interviews.
Swine Flu

Class presentation materials will be made available on the course web site. If you are sick, stay home and don’t infect anyone else.
The only stupid question is one you don’t ask.

“Better to keep your mouth shut and be thought a fool than to open it and remove all doubt.” -- Mark Twain
Homework

- Review ECE 320 material, prepare for assessment test
- Read Palnitkar through Chapter 2
- Read Lab Manual through Experiment 1
- Make sure you have access to your UNIX account
- No deliverables this week
What’s an ASIC, Anyhow?

• Application Specific Integrated Circuit
  – Processors are generally NOT considered ASIC though design methodology is essentially identical. Processors (including DSP’s) are multi-purpose devices.
• Pretty much all integrated circuits are developed using ASIC methodology.
• Many times more ASIC’s are designed every year than GP Processors.
ASIC Classes

- Custom Mask
  - Full Custom
  - Standard Cell
- FPGA
  - Gate Array
    - Structured
    - Unstructured
It’s a Hot Field

- **Brief** | **Detailed** | View jobs on map
- Results 1-25 of 350  Next »
- **ASIC ENGINEER POSITION-OPPORTUNITY OF A LIFETIME!!** The Select Group
  Raleigh, NC 27607  Aug 20
  ASIC ENGINEERS - Multiple Positions! Our client, new to the Raleigh market and growing rapidly, has won numerous awards and is ready to make their mark here in the Triangle!!! They are working with gr ... More
- **Senior ASIC Design Verification Engineer** Cisco Systems
  San Jose, CA 95134  Aug 20
  We are seeking a Senior ASIC Design Engineer with specialized knowledge in digital ASIC design and networking technologies to join in the design of the Next Generation ASICs for our Catalyst 4K produc ... More
- **ASIC Design Engineer** CyberCoders
  Los Angeles 90001  Aug 20
  Location Los Angeles, CA; Long Beach, CA Salary $90,000 - $110,000 Education Bachelor of Science Category Engineering Experience Required At least 2 Years Short Description ASIC Engineer - VHDL or Ver ... More
- **SR SoC/ASIC Designer** SemiconductorTalent.com
  Portland, OR 97201

More every day: Monster search done Aug. 20.
Digital Design

• Virtually all digital design is now done in ASICs.
• Virtually all ASICs are designed using an HDL and logic synthesis.
• Verilog is the HDL of choice among most engineers and companies, particularly in California.
• A few use VHDL.
Karnaugh Map

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Minimize Functions Manually

Sometimes it takes a few tries to find the best implementation.
“Best” design may be smallest, fastest, lowest power, quickest to market. Any one design will not be best in all categories.
Redundancy For Reliability

The smallest design might not be the most desirable.
Four-bit Counter

Pin numbers shown are for D, J, N, and W packages

Image © Texas Instruments
Encode States (half table shown)

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Manual Minimization Limits

• Anyone can make a K-map for 4 inputs.
• 5 inputs is a bit tedious, but still manageable. Beyond 6?
• Useful devices tend to have a lot of states and inputs.
• Sum of products may not be the best implementation.
• Consider something so basic as a stoplight controller—pretty simple compared to a Pentium-class processor.
Stoplight Controller

- States: Red, Yellow, Green for each direction.
- Left-turn arrows: maybe 4, maybe 8
- Right-turn arrows: maybe 4
- Pedestrian lights: several possible states
- Sensors: push buttons and magnetic detectors
- Emergency Services override
- Fail-safe mode
- Once a single controller is perfect, synchronize it with the rest of the city.
Moore’s Law

2005: “Cell” processor has 234 million transistors
2006: Intel produces 153 megabit SRAM with > 1 billion transistors
2007: “Peryn” dual-core has 410 million, quad-core will have 820

Who is going to design all those gates?
Engineering Density in the USA
EDA : Electronic Design Automation

The process of using computer-based software systems to design very large-scale integrated (VLSI) circuits.

All modern integrated circuits are designed with EDA tools.

This course uses Verilog HDL for hardware description and the NC Verilog simulator from Cadence for simulation.
Course Outline

1. Introduction to EDA (Electronic Design Automation).
2. Introduction to Hardware Modeling
3. Verilog primitive operators and structural modeling
4. Design verification: folded into other topics
5. Synchronization and synchronous design
6. Top down and bottom up methodology
7. Library modeling