Part VIII
Overall Concept on VHDL
VHDL is a Standard Language

- Standard in the electronic design community.
- VHDL will virtually guarantee that you will not have to throw away and re-capture design concepts simply because the design entry method you have chosen is not supported in a newer generation of design tools.
- Takes advantage of the most up-to-date design tools, and will have access to a knowledge-based of thousands of other engineers, many of who are solving problems similar to your own (Model availability).
- Tool interoperability
- Design Documentation
VHDL is “Strongly Typed”

- In VHDL information (objects) must be of a type.
- The type specifies the values the object may have.
- Users may also define their own data types and operators.
- Vendors provide extended data types for simulation and synthesis.
VHDL is a Design Entry Language

- VHDL allows the behavior of complex electronic circuits to be captured into a design system for automatic circuit synthesis or for system simulation.

- Like Pascal, C and C++, VHDL includes features useful for structured design techniques, and offers a rich set of control and data representation features.

- Unlike these other programming languages, VHDL provides features allowing concurrent events to be described. This is important because the hardware being described using VHDL is inherently concurrent in its operations.
VHDL is a Simulation Modeling Language

- VHDL has many features appropriate for describing (to an excruciating level of detail) the behavior of electronic components ranging from simple logic gates to complete microprocessors and custom chips.

- VHDL allows electrical aspects of circuit behavior (such as rise and fall times of signals, delays through gates, and functional operation) to be precisely described.

- The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams or system-level VHDL descriptions) for the purpose of simulation.

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VHDL is a Test language

- An important (and under-utilized) aspects of VHDL is its ability to capture the performance specification for a circuit, in a form commonly referred to as a test bench.

- Test benches are VHDL descriptions of circuit stimulus and corresponding expected outputs that verify the behavior of a circuit over time.

- Test benches should be an integral part of any VHDL project, test benches are portable.

- Should be created in parallel with other descriptions of the circuit.
VHDL for Simulation

- Purely behavioral
- Architectural: bus widths, number of processors
- Off-the-shelf components
- Test benches

VHDL Source Code

entity processor is
    ....
end processor;

Simulation Output
VHDL for Synthesis

- RTL description => Synthesis Compiler => Gates (LSI, TI)
- Simulate RTL description for functionality
- Simulate gates for timing and to check synthesis
- Target a synthesis tool from the start
- Logic model, used to simulate ASIC in any environment

```
VHDL Source File

entity processor is
   ..... 
end processor;
```
VHDL is a Netlist Language

- VHDL is a powerful language with which to enter new designs at a high level.

- Also useful as a low-level form of communication between different tools in a computer-based design environment.

- VHDL’s structural language features allow it to be effectively used as a netlist language, replacing (or augmenting) other netlist languages such as EDIF.
VHDL for Gate-Level Simulation

- VITAL - Vital Initiative Towards ASIC Libraries
- SDF - Standard Delay Format for back annotation (Internal layout tools already have this)
- Gates take longer to simulate and more money
- Can simulate on non-VHDL platforms also such as in Mentor
- VHDL looks like other netlist formats
VHDL for Documentation /Translation

- Used to transfer designs between contractor and subcontractor
- Re-use of designs parts, utilities
- Many vendors take in and produce VHDL
- Quite readable
A complete VHDL component description requires a VHDL entity and a VHDL architecture.

- The entity defines a component’s interface
- The architecture defines a component’s function

Several alternative architectures may be developed for use with the same entity.

Three areas of description for a VHDL component:

- Structural descriptions
- Behavioral descriptions
- Timing and delay descriptions
Fundamental unit for component behavior description is the process
- Processes may be explicitly or implicitly defined and are packaged in architectures

Primary communication mechanism is the signal
- Process executions result in new values being assigned to signals which are then accessible to other processes
- Similarly, a signal may be accessed by a process in another architecture by connecting the signal to ports in the the entities associated with the two architectures
- Example signal assignment statement: `Output <= My_id + 10;`
Packages and Libraries Used in VHDL Modeling

- VHDL is a hardware description language used to document an electronic system design.

- VHDL consists of several parts organized as follows:
  - The actual VHDL Language
  - Some additional data type declarations in the Package STANDARD
  - Some utility functions in the Package TEXTIO
  - A Work Library reserved for personal designs
  - A STD library containing Package STANDARD and TEXTIO
  - A vendor package
  - Vendor Libraries
  - User libraries and packages
Designing in VHDL

Front end entry/swap level

Concept

Architecture

Algorithm (Behavioral)

Register Transfer Level

Gate Level Description (netlist)

Reverse Synthesis
Real World Design Flow

- Model design using RTL - synthesis tool specific
- Simulate each hierarchical block
- Thoroughly test full RTL design for functionality using VHDL test bench(es)
- Write (instantiate the ASIC into another level of VHDL environment.) Test bench is portable to other vendors. Behavioral wrapper around the ASIC.
- Synthesize RTL description
- Simulate gate-level description in VHDL simulator or Gate-level (non-VHDL) simulator.
The FPGA/AISC Design Process

- Design Entry
- Synthesis
- Device Mapping
- Device
- Test Development
- Functional Simulation
- Timing Simulation

VHDL can be used for both design and test development.
ASIC Design Flow

Functional Steps

RTL Coding

Behavioral Simulation

Logic Synthesis

Test Insertion / ATPG

Netlist Simulation

Floor Panning Place and Route

In-Place Optimization

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