EE 595

Part III
Simulation and Timing in VHDL
Simulation Cycle in VHDL

First-Generation simulators used a technique CAD developers call a one-list algorithm, which is relatively fast but cannot handle parallel zero delay events such as exchanging \( A \) and \( B \).

\[
\begin{align*}
A &\leq B; \quad \text{zero delay} \\
B &\leq A; \quad \text{zero delay}
\end{align*}
\]

This example would not exchange the values of \( A \) and \( B \), but would give both \( A \) and \( B \) the old value of \( B \), using one-list algorithm.

VHDL uses a \textit{two-list algorithm}, which tracks the previous and new values of signals. In this method, expressions are first evaluated, then signals are assigned new values. In VHDL, the example code performs a data exchange between the two signals \( A \) and \( B \) at some point in simulation time. In operation, the old values of \( A \) and \( B \) are fetched and scheduled for assignment, for zero delay, after a subsequent WAIT statement is executed.
Simulation Cycle in VHDL (cont’d)

The ordering of zero delay events is handled with a fictitious unit called *delta time*. Delta time represents the execution of a simulation cycle without advancing Simulation time.

All right-hand side assignments (evaluations) are calculated after assignments are made.

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The key points of simulation and delta time are:

- The simulator models zero-delay events using delta time.
- Events scheduled at the same time are simulated in specific order during a delta time step.
- Related logic is then re-simulated to propagate the effects for another delta time time step.
- Delta time steps continue until there is no activity for the same instant of simulated time.
Timing Model of VHDL Simulation Cycle

- VHDL uses a simulation cycle to model the stimulus and response nature of digital hardware.
Delay Types

- All VHDL signal assignment statements prescribe an amount of time that must transpire before the signal assumes its new value.

- This prescribed delay can be in one of three forms:
  - **Transport** -- prescribes propagation delay only
  - **Inertial** -- prescribes minimum input pulse width and propagation delay
  - **Delta** -- the default, if no delay time is explicitly specified
Transport Delay

- Delay must be explicitly specified by user
  - Keyword “TRANSPORT” must be used
- Signal will assume its new value after specified delay

```plaintext
-- TRANSPORT must be specified
Output <= TRANSPORT NOT (Input) AFTER 10 ns;
```
Inertial Delay

- Provides for specification of input pulse width, i.e. ‘inertia’ of output, and propagation delay:

  \[ \text{target} \leq [\text{REJECT time\_expression}] \text{INERTIAL waveform}; \]

- Inertial delay is default and REJECT is optional:

  \[ \text{Output} \leq \text{not(Input)} \text{ after 10 ns}; \]
  -- Propagation delay and minimum pulse width are 10ns
Inertial Delay (cont’d)

- Example of gate with ‘inertia’ smaller than propagation delay
  - e.g. Inverter with propagation delay of 10ns which suppresses pulses shorter than 5ns

```
Output <= REJECT 5ns INERTIAL not(Input) after 10ns;
```

![Graph showing input and output signals with time intervals 0 to 35]

- Note that *REJECT* feature is new to VHDL 1076-1993
Delta Delay

- Default signal assignment propagation delay if no delay is explicitly prescribed
  - VHDL signals assignment cannot take place immediately
  - Delta is an infinitesimal VHDL time unit so that all signal assignments can result in signals assuming their values at some future time
  - E.g.

```vhdl
Output <= not(Input);
-- Output assumes new value in one delta cycle
```

- Supports a model of concurrent VHDL process execution
  - The order in which processes are executed by simulator does not affect simulation output
Delta Delay
An Example Without Delta Delay

- What is the behavior of C?

IN: 1->0

NAND gate evaluated first:
- IN: 1->0
- A: 0->1
- B: 1->0
- C: 0->0

AND gate evaluated first:
- IN: 1->0
- A: 0->1
- C: 0->1
- B: 1->0
- C: 1->0
Delta Delay
An Example With Delta Delay

- What is the behavior of C?

Using delta delay scheduling

<table>
<thead>
<tr>
<th>Time</th>
<th>Delta</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 ns</td>
<td>IN: 1-&gt;0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>eval INVERTER</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>A: 0-&gt;1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>eval NAND, AND</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>B: 1-&gt;0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C: 0-&gt;1</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>eval AND</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>C: 1-&gt;0</td>
</tr>
<tr>
<td></td>
<td>1 ns</td>
<td></td>
</tr>
</tbody>
</table>

IN: 1->0

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Transport Versus Inertial Delay

- Inertial Delay
  - Default in VHDL
  - Can be similar to actual device behavior
  - Spikes are “swallowed”
  - Most commonly used in simulator

- Transport Delay
  - Must specify with key word TRANSPORT
  - Ideal delay, passes any width pulse
  - Good for wire delay and time modeling.
Delta Time

- Delta Time is a simulation time cycle. It is used to order sequential events during simulation. More than one event can occur during a delta time.

- The time between any two sequential events is called a delta. These two events may be happening at the same real time but in a specific order, or they may be separated by a large real time during which time the circuit has been “quiet”.

- A delta is the default value or if zero delay is specified as in:
  
  ```
  A <= not B;
  ```

  These are the same as:
  
  ```
  A <= not B after 0 ns;
  ```
A combinational Circuit, in which all elements have zero delay, would settle down in 0 ns, but could occupy many deltas.