Introduction to Xilinx
Who is Xilinx?

- World’s leading innovator of complete programmable logic solutions
- Inventor of the Field Programmable Gate Array
- Fabless Semiconductor and Software Company
  - UMC (Taiwan) (*Xilinx acquired an equity stake in UMC in 1996)
  - Seiko Epson (Japan)
  - TSMC (Taiwan)
Electronic Components

Source: Dataquest

Logic

Standard Logic

ASIC

Programmable Logic Devices (PLDs)

Gate Arrays

Cell-Based ICs

Full Custom ICs

Gate Arrays

Common Resources

Configurable Logic Blocks (CLB)

- Memory Look-Up Table
- AND-OR planes
- Simple gates

Input / Output Blocks (IOB)

- Bidirectional, latches, inverters, pullup/pulldowns

Interconnect or Routing

- Local, internal feedback, and global

SPLD = Simple Prog. Logic Device
PAL = Prog. Array of Logic
CPLD = Complex PLD
FPGA = Field Prog. Gate Array
Programmable Logic Solution

• No high development cost barriers
• Recovered time for authoring and innovating
  – SW improvements reduce design iterations
• No lengthy prototyping cycle
• Ability to remotely upgrade any networked system
• Ultimate flexibility to manage rapid change
Xilinx Products

CPLDs and FPGAs

Complex Programmable Logic Device (CPLD)

Field-Programmable Gate Array (FPGA)

Architecture
- PAL/22V10-like
- More Combinational
- Gate array-like
- More Registers + RAM

Density
- Low-to-medium
- 0.5-10K logic gates
- Medium-to-high
- 1K to 8M system gates

Performance
- Predictable timing
- Up to 250 MHz today
- Application dependent
- Up to 420 MHz today

Interconnect
- “Crossbar Switch”
- Incremental
Xilinx Products
Design Tools

V5.1i ISE Software

- Complete Software Package
  - Design Entry (Schematic, VHDL, Verilog)
  - Synthesis (XST)
  - Implementation (Translate, Map, Place & Route)
  - Simulation (ModelsimXE-II)
  - iMPACT Programmer (Download Bistream)

- CORE Generator
  - Parameterizable Cores

- StateCAD/State Bencher
  - State Machine Design

- HDL Bencher
  - Test Bench Generation

- Unix & PC Platforms
5.1i Device Support

*all Xilinx leading FPGA/CPLD families*

- New leading-edge device families

![Device Logos]

- ISE advantages can be leveraged across various Engineering courses
  - Across all device families and design sizes
Programmable Logic Design Flow

1. **Design Entry** in schematic, ABEL, VHDL, and/or Verilog.

2. **Implementation** includes Placement & Routing and bitstream generation using Xilinx’s M1 Technology. Also, analyze timing, view layout, and more.

3. **Download** directly to the Xilinx hardware device(s) with unlimited reconfigurations*!!
## Xilinx Programmable Logic in your Curriculum

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<th>Density</th>
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<td>Up to 300K System Gates</td>
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<td>Virtex-II</td>
<td>40K to 8M System Gates + up to 168 Multier Blocks</td>
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<td>Virtex-II Pro</td>
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