Global Timing Constraints
Objectives

After completing this module, you will be able to...

- Apply timing constraints to a simple synchronous design
- Specify global timing constraints and pin assignments with the Constraints Editor
Outline

- Introduction
- The Period Constraint
- The Offset Constraint
- The Constraints Editor
- Summary
What Effects Do Timing Constraints Have on Your Project?

- The Implementation tools don’t try to find the place and route that will obtain the best speed
- Instead, the Implementation tools try to meet your performance expectations
- Performance expectations are communicated with timing constraints
- Timing Constraints improve the design performance by placing logic closer together so shorter routing resources can be used
- Note that when we discuss using the Constraint Editor, we are referring to the Design Manager Constraints Editor
Without Timing Constraints

- This design had no timing constraints or pin assignments entered when it was implemented.
- Note the logical structure of the placement and pins.
- Xilinx recommends that you compile your design at least once without timing constraints or pin assignments.
- This design has a maximum system clock frequency of 50 MHz.
With Timing Constraints

- This is the same design with three global timing constraints entered with the Constraints Editor.
- It has a maximum system clock frequency of 60 MHz.
- Note how most of the logic is placed closer to the edge of the device where the pins have been placed.
More About Timing Constraints

- Timing constraints should be used to define your performance objectives
  - Specifying tight timing constraints will increase your compile time
  - Specifying unrealistic constraints will cause the Flow Engine to stop
  - Use the Logic Level Timing Report to determine if your constraints are realistic
  - After implementing your design, review the Post Layout Timing Report to determine if your design performance objectives were met
- If your constraints were not met, use the Timing Analyzer to determine the cause
Path End Points

- Timing constraints optimize delay paths between path endpoints. Path endpoints can be **pads**, **flip-flops**, **latches**, and **RAMs**.

- Timing constraints create **groups of path endpoints** and communicate a timing specification between these groups.

- Since delay paths may require signals to go through multiple function generators in series, optimizing between path endpoints requires the Implementation tools to place logic closer together.
Review Questions

Global constraints cover multiple delay paths with a single line of text created by the Constraints Editor. A single global constraint in this example will improve 3 paths.

- If the arrows are constrained paths, what are the Path End Points in this circuit? Do all of the registers have anything in common?

![Diagram of digital circuit with ADATA, CLK, BUFG, BUS [7..0], CDATA, FLOPs, OUT1, and OUT2 nodes connected in various paths, with the text "= Combinatorial Logic" at the bottom right.]
Answers

- If the arrows are constrained paths, what are the Path End Points in this circuit?
  - The Path End Points are flip-flops

- Do all of the registers have anything in common?
  - The registers are all clocked by the same signal. A constraint that references this net could constrain all delay paths between all of the registers in the design
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Period Constraint

- The Period constraint optimizes all delay paths between flip-flops

- The Period constraint does NOT optimize delay paths from input pads to output pads (purely combinatorial), paths from input pads to flip-flops, or paths from flip-flops to output pads
The Period Constraint

- A synchronous element is a flip-flop, latch, or a synchronous RAM

- The Period constraint covers paths...
  - Between synchronous elements which are clocked by the reference net

- Synchronous elements are grouped by the clock signal driving them. This is called forward propagation and enables constraining large pieces of logic with a single constraint
Some Features of the Period Constraint

- The PERIOD constraint automatically accounts for the extra delay caused by inverters and global clock buffers placed on clock signals
  - This provides the most accurate timing information
- The PERIOD constraint automatically accounts for unequal clock duty cycles
- Assume:
  - 50% duty signal on CLK
  - Period of 20ns
  - Since FF2 will be clocked on the falling edge of CLK, the delay between the two flip-flops will actually be constrained to 20ns - 10ns = 10ns
The Pad-to-Pad Constraint

- Purely combinatorial delay paths do not contain any synchronous elements
- Purely combinatorial delay paths start and end at I/O pads and are often left unconstrained by users
- Placing a Pad-to-Pad constraint is essential for completely constraining a design
Skills Check
Questions

- Which paths are constrained by a PERIOD constraint on CLK1?
- Which paths are constrained by a Pad-to-Pad constraint?
Answers

- Which paths are constrained by a PERIOD constraint on CLK1?
  - FLOP to LATCH

- Which paths are constrained by a Pad-to-Pad constraint?
  - PADC to OUT2
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Offset Constraint

- The Offset constraint optimizes delay paths from input pads to flip-flops and paths from flip-flops to output pads

Offset In

Offset Out

Combinatorial Logic
The Offset Constraint

- The Offset constraint covers paths...
  - From input pads to synchronous elements clocked by the reference net (Offset In)
  - From synchronous elements to output pads clocked by the reference net (Offset Out)

- Note, that this constraint does not cover paths...
  - Between synchronous elements
  - From pads to pads (purely combinatorial paths)
Some Features of the Offset Constraint

- The OFFSET constraint automatically accounts for the extra delay caused by inverters and global clock buffers placed on clock signals
  - This provides the most accurate timing information
  - This increases the amount of time for input signals to arrive at synchronous elements
  - This reduces the amount of time for output signals to arrive at output pins
Question

- Which paths are constrained by an Offset In and Offset Out constraint in this circuit?
Answer

- Which paths are constrained by an Offset In and Offset Out constraint in this circuit?
  - Offset In: PADA to FLOP and PADB to RAM
  - Offset Out: LATCH to OUT1, LATCH to OUT2, and RAM to OUT1
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Starting the Constraints Editor

- If you are using the Alliance version, start the Constraints Editor by using the command...
  - Utilities -> Constraints Editor from the Design Manager
Making Pin Assignments with the Ports Tab

- Pad locations and Slew Rate can be assigned on a pin-by-pin basis
- Place pin assignments late in the design cycle
  - Early pin locking can make obtaining performance objectives more difficult
- To make Pin Assignments, double-click on the appropriate box under the Location heading
- Then type “P60” to assign the signal to Pin 60 of the device
Making Pin Assignments with the Ports Tab

- Prohibit I/O Locations when saving pins for a team design project
- Prohibiting is also useful for handling dual-purpose pins, such as configuration pins
Making Period and Pad-to-Pad Constraints with the Global Tab

- Clock Periods can be made by clicking on the Global tab and specifying a period length for each clock signal.

- Double-click here to make a period constraint.

- A global Pad-to-Pad constraint can be entered here.
Period Constraint Options

- After double-clicking under the Period heading, the Clock Period dialog box opens
- This allows customizing the constraint to the duty-cycle and rising or falling clock edge
- It is also possible to place timing constraints relative to other timing constraints. This is useful for designs with multiple clock signals and multi-cycle paths
Making Offset Constraints with the Constraints Editor

- Global Offset IN/OUT constraints can be made by clicking on the Global tab
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Review Question

- If...
  
  the internal delay on an input signal ADD0_IN is **14 ns**, the internal delay on the output ADD0_OUT is **12 ns**, and the design should perform with a period of **40 ns**...

- What constraints should be placed in the Constraints Editor?

```
ADD0_IN
```

```
CLK
```

```
FF1
```

```
FF2
```

```
ADD0_OUT
```

40ns

Determined by Software

T_input = 14ns

Determined by Software

T_output = 12ns
Answer

- What constraints should be placed in the Constraints Editor?
Summary

- Performance expectations are communicated with timing constraints

- The PERIOD constraint improves delay paths between synchronous elements

- The OFFSET constraint improves delay paths from input pins to synchronous elements, and paths from synchronous elements to output pins

- The Constraints Editor allows you to create timing constraints
Lab 5: Global Timing Constraints

- Apply the PERIOD and OFFSET constraints
- Analyze the effect of the constraints on the design