Architecture
Spartan-IIIE Technical Details

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- Embedded Memory
- System Clock Management
- Interfaces – Select I/O
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The Spartan-IIE Solution
More Than Just Silicon

I/O Connectivity
SelectIOTM Technology
Support major I/O standards

Logic & Routing
Flexible logic implementation
Vector Based Routing
Internal 3-State bussing

Memory Resources
SRL16 registers
Distributed Memory
Block Memory
External Memory

System Clock Management
Digital Delay Lock Loops (DLLs)
Spartan-IIIE Features

- System Clock Management
- Embedded Memory
- System Interfaces
- Logic & Routing

Configuration
Spartan-IIE Features

Logic & Routing
Logic & Routing

- Configurable for simple to complex logic
- Excellent for fast arithmetic operations
- Flexible for logic or distributed RAM implementations

- Predictable routing delays
- Core-friendly architecture
- Quick Place and Route times
- Internal 3-state bussing
Logic Advantages

- Look Up Table (LUT) versatility
  - CLB primary building block
  - Flexible for logic or distributed RAM implementation

- Fast arithmetic operations
  - Specialized Carry Logic for arithmetic operations
  - Fast DSP functions FIR filters

- Configurable for simple to complex logic
  - Allow up to 6 input functions into a one logic level
- Each slice has 2 LUT-FF pairs with associated carry logic
- Two 3-state buffers (BUFT) associated with each CLB, accessible by all CLB outputs
CLB Slice Structure

• Each slice contains two sets of the following:
  – Four-input LUT
    • Any 4-input logic function
    • Or 16-bit x 1 sync RAM
    • Or 16-bit shift register
  – Carry & Control
    • Fast arithmetic logic
    • Multiplier logic
    • Multiplexer logic
  – Storage element
    • Latch or flip-flop
    • Set and reset
    • True or inverted inputs
    • Sync. or async. control
**Four-Input LUT**

- Implements combinatorial logic
  - Any 4-input logic function
  - Cascaded for wide-input functions

<table>
<thead>
<tr>
<th>Inputs (ABCD)</th>
<th>Output (Z)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0</td>
</tr>
<tr>
<td>0001</td>
<td>0</td>
</tr>
<tr>
<td>0010</td>
<td>1</td>
</tr>
<tr>
<td>0011</td>
<td>0</td>
</tr>
<tr>
<td>.............</td>
<td>..</td>
</tr>
<tr>
<td>1110</td>
<td>1</td>
</tr>
<tr>
<td>1111</td>
<td>1</td>
</tr>
</tbody>
</table>

4-input logic function
Dedicated Expansion Multiplexers

- MUXF5 combines 2 LUTs to create
  - 4x1 multiplexer
  - Or any 5-input function (LUT5)
  - Or selected functions up to 9 inputs
- MUXF6 combines 2 slices to form
  - 8x1 multiplexer
  - Or any 6-input function (LUT6)
  - Or selected functions up to 19 inputs
- Dedicated muxes are faster and more space efficient
Distributed RAM

- CLB LUT configurable as Distributed RAM
  - A LUT equals 16x1 RAM
  - Implements Single and Dual-Ports
  - Cascade LUTs to increase RAM size
- Synchronous write
- Synchronous/Asynchronous read
  - Accompanying flip-flops used for synchronous read
Shift Register

- Each LUT can be configured as shift register
  - Serial in, serial out
- Dynamically addressable delay up to 16 cycles
- For programmable pipeline
- Cascade for greater cycle delays
- Use CLB flip-flops to add depth
Shift Register

- Register-rich FPGA
  - Allows for addition of pipeline stages to increase throughput
- Data paths must be balanced to keep desired functionality
Shift Register

- LUT as shift register
  - Used to add pipeline stages
- Increase overall register count
  - 16 bit shift register per LUT
  - 64 bit shift register per CLB

Paths statically balanced
CLB Arithmetic Logic

- Dedicated carry logic
  - Provides high performance for counters & arithmetic functions
  - Discrete XOR component for single level sum completion
  - Two separate carry chains in CLB allow for 3 operand functions
  - Can also be used to cascade LUTs for wide-input logic functions
3 Operand Adder Function

- A, B, C are two-bits wide
  - SUM = A + B + C or PARTIAL + C, where PARTIAL = A + B
  - Implementation
    - First 2-operand sum ‘A+B’ is performed in Slice 0
    - Second 2-operand sum ‘PARTIAL + C’ is performed in Slice 1
  - Fast local feedback connection within the CLB
    - Very small delay for on PARTIAL
Carry Logic for Wide Input Functions

- Higher performance
- Efficient resource utilization
- Common applications
  - Wide input decoding
  - Comparators
- HDL design entry
  - LUT can be inferred
  - MUXCY must be instantiated
12- Input AND Function

4-Input AND Truth Table

<table>
<thead>
<tr>
<th>Inputs(ABCD)</th>
<th>Output(Z)</th>
<th>Output(HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0001</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0010</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0011</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>1011</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>1101</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1110</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1111</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

- **Utilization**
  - 3 LUTs and 3 MUXCYs
  - As opposed to 4 LUTs
- **Performance**
  - 1 logic level
  - As opposed to 2 logic levels
12- Input OR Function

4-Input NOR Truth Table

<table>
<thead>
<tr>
<th>Inputs(ABCD)</th>
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<tbody>
<tr>
<td>0000</td>
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<td></td>
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<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0010</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0011</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>......</td>
<td>......</td>
<td>...</td>
</tr>
<tr>
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<td>0</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1101</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td></td>
</tr>
<tr>
<td>1111</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

- **Utilization**
  - 3 LUTs and 3 MUXCYs
  - As opposed to 4 LUTs

- **Performance**
  - 1 logic level
  - As opposed to 2 logic levels
Dedicated CLB Multiplier Logic

- Dedicated AND gate
- Highly efficient ‘Shift & Add’ implementation
  - For a 16x16 Multiplier
    - 30% reduction in area and one less logic level
Lower Operating Power

• 1.8V core supply
  – Reduces power consumption
• Advanced signaling standards
  – Smaller voltage transitions
  – Reduces switching power
• DLLs reduce clock speed requirements
  – Faster clock propagation
  – Internal multiplication of clock
  – Reduces power on clock nets
Logic Summary

• Flexible Configurable Logic Block (CLB) implementations
  – Logic
  – Distributed RAM
  – Shift register

• CLB configurable for simple to complex logic
  – Any 6 input function into one logic level

• Excellent for fast arithmetic operations
  – Specialized carry logic for arithmetic operations
  – Fast DSP functions FIR filters
Spartan-IIIE Features

Logic & Routing
Routing

• **Core-friendly vector-based routing**
  – Provides predictable routing delays independent of
    • IP placement
    • Number of IP
    • Device size

• **Superior routing**
  – Quick Place and Route times
    • Design to system at 100,000 gates per minute
  – Easier rerouting

• **Internal 3-state bussing**
  – Eliminates bus routing contention
  – Reduced CLB usage by using 3 states instead of MUXs
  – Increases performance by reducing logic levels
High-Performance Routing

- Local routing
  - Direct connections
- General Routing Matrix (GRM)
  - Single line, Long line, Hex line
- Dedicated routing
  - Internal 3-state bus
- Global routing
  - Primary Clock Buffer lines, Secondary lines
Local Routing

- Interconnect among LUTs, FFs, GRM
- CLB feedback path for connections to LUTs in same CLB
- Direct path between horizontally adjacent CLBs
General Purpose Routing

- 24 single-length lines
  - Route GRM signals to adjacent GRMs in 4 directions
- 96 buffered hex lines
  - Route GRM signals to another GRMs six blocks away in each of the four directions
- 12 buffered Long lines
  - Routing across top and bottom, left and right
Routing Summary

• Vector-based routing
  – Predictable routing delays independent of device size and routing direction
• Core-friendly architecture
• Quick Place and Route times
  – Design to system at 100,000 gates per minute
  – Easier re-routing
• Internal 3-state bussing
  – Eliminates bus routing contention
  – Improves density and performance
Spartan-IIIE Features

- Embedded Memory
Spartan-IIE Memory Hierarchy

Shift Register LUT
- 16 registers, 1 LUT
- Compact & fast

Distributed RAM
- Single-port
- Dual port
- Cascadable

Block RAMs
- 4Kbit blocks
- True dual-port

High-Performance External Memory Interfaces
- DDR I/O
- SSTL, HSTL, CTT

Shift Register LUT
- 16 registers, 1 LUT
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- Dual port
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Block RAMs
- 4Kbit blocks
- True dual-port

Bytes

Kilobytes

Megabytes

SDRAM
SGRAM
PB SRAM
DDR SRAM
ZBT SRAM
QDR SRAM

• Collaboration with memory vendors
  • IDT, Cypress, Micron, NEC, Samsung, Toshiba...

For Academic Use Only
Distributed RAM

- CLB LUT configurable as Distributed RAM
  - A LUT equals 16x1 RAM
  - Implements single and dual ports
  - Cascade LUTs to increase RAM size
- Synchronous write
- Synchronous/Asynchronous read
  - Accompanying flip-flops used for synchronous read
SRL-16 and SRL-16E

16-bit Shift Register Look-Up-Table

16-bit Shift Register Look-Up-Table with Clock Enable

For Academic Use Only
Distributed RAM
Dual-Port Implementation

- 2 LUTs equal 16x1 dual-port RAM
- A Port
  - Uses A[3:0] address
  - Write and read
- B Port
  - Uses DPA[3:0] address
  - Read only
- Excellent for FIFOs, scratch pads....
Block RAM

• Most efficient memory implementation
  – Dedicated blocks of memory

• Ideal for most memory requirements
  – 8 to 72 memory blocks
    • 4096 bits per blocks
  – Use multiple blocks for larger memories

• Builds both single and true dual-port RAMs

• CORE Generator provides custom-sized block RAMs
  – Quickly generates optimized RAM implementation
Block RAM

• Configurable synchronous Block RAM
  – Single-port RAM
  – True dual-port RAM
  – Two independent single-port RAMs

• Block count increases with FPGA size

<table>
<thead>
<tr>
<th>Device</th>
<th>No. of Blocks</th>
<th>Block RAM Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC2S50E</td>
<td>8</td>
<td>32,768</td>
</tr>
<tr>
<td>XC2S100E</td>
<td>10</td>
<td>40,960</td>
</tr>
<tr>
<td>XC2S150E</td>
<td>12</td>
<td>49,152</td>
</tr>
<tr>
<td>XC2S200E</td>
<td>14</td>
<td>57,344</td>
</tr>
<tr>
<td>XC2S300E</td>
<td>16</td>
<td>65,536</td>
</tr>
<tr>
<td>XC2S400E</td>
<td>40</td>
<td>163,840</td>
</tr>
<tr>
<td>XC2S600E</td>
<td>72</td>
<td>294,912</td>
</tr>
</tbody>
</table>
Block RAM

- Flexible 4096-bit block... Variable aspect ratio
  - 4096 x 1
  - 2048 x 2
  - 1024 x 4
  - 512 x 8
  - 256 x 16

- Increase memory depth or width by cascading blocks
Block RAM
Single-Port Implementation

- Easy cascading of block RAMs
- Utilize variable aspect ratio for desired RAM size
- Example
  - Desired RAM size: 1024 x 8
  - 1024 x 4 + 1024 x 4 = 1024 x 8
- CORE Generator software
  - Efficiently cascades RAM blocks
  - Quick custom RAM implementation
Dual-Port Bus Flexibility

- Each port can be configured with a different data bus width
- Provides easy data width conversion without any additional logic
Two Independent Single-Port RAMs

- Added advantage of True Dual-Port
  - No wasted RAM Bits
- Can split a Dual-Port 4K RAM into two Single-Port 2K RAM
  - Simultaneous independent access to each RAM

- To access the lower RAM
  - Tie the MSB address bit to Logic Low
- To access the upper RAM
  - Tie the MSB address bit to Logic High
CAM in Block RAM

- Content Addressable Memory (CAM)
  - Storage array like a RAM
  - Functionally opposite of a RAM
    • Quickly find the location of a particular stored value
    • Output the address and toggle the MATCH line, if data match is found

- Used in telecommunications, networking, Ethernet, ATM switches
- Xilinx provides reference designs and application notes
External Memory Interface

- Easy access to high-speed external memory
- SelectI/O™ provides interface to most memory types

<table>
<thead>
<tr>
<th>External Memory Type</th>
<th>SelectI/O Standard</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>SSTL</td>
</tr>
<tr>
<td>SGRAM</td>
<td>HSTL</td>
</tr>
<tr>
<td>ZBT SRAM/NoBL</td>
<td>LVTTL</td>
</tr>
<tr>
<td>QDR SRAM</td>
<td>HSTL</td>
</tr>
<tr>
<td>SDRAM</td>
<td>LVTTL</td>
</tr>
<tr>
<td>DDR SRAM</td>
<td>SSTL2</td>
</tr>
<tr>
<td>EDO</td>
<td>TTL</td>
</tr>
<tr>
<td>FPM</td>
<td>TTL</td>
</tr>
<tr>
<td>PB</td>
<td>TTL</td>
</tr>
<tr>
<td>PC100/133</td>
<td>LVTTL / SSTL</td>
</tr>
</tbody>
</table>
Memory Controller Designs
Memory Resources

- DRAM controller
  - 64-bit DDR DRAM controller
  - 16-bit DDR DRAM controller
  - SDRAM controller
- SRAM controller
  - ZBT SRAM controller
  - QDR SRAM controller
  - SigmaRAM controller
- Flash controller
  - NOR / NAND flash controller
- Embedded memory
  - CAMs, FIFOs

- Memory Solutions Portal
- [www.xilinx.com/memory](http://www.xilinx.com/memory)

Download Now!
Embedded Memory
Summary

• Fast distributed RAM
  – Data right beside logic
• Memory requirements solved by Block RAM
  – Single and True Dual-Port RAM implementations
  – FIFO for buffering data
  – Data width conversion
  – Cache
  – Register stacks
  – CAM for high-speed parallel searches
  – Many more
• Direct connection to external high-speed memory
Spartan-IIIE Features

System Clock Management
System Clock Management

- 100% Digital DLL Design
  - Noise insensitive
  - Scalable to new processes
  - Excellent Jitter specifications
    - +/- 100ps, <<50ps Typical
    - No cumulative phase error
  - Used in advanced memories

- Every Spartan-IIE device has
  - 4 DLLs
  - External clock outputs

"Delay Locked Loops Lower Board Costs"
System Clock Management

Delay Lock Loops (DLLs) Lower Board Costs
Generic DLL Operation

- A DLL inserts delay on the clock net until the clock input rising edge is in phase with the clock feedback rising edge.
- Requires a well-designed clock distribution network: the clock edges arrive simultaneously everywhere in the part.
DLL Capabilities

- Easy clock duplication
  - System clock distribution
  - Cleans and reconditions incoming clock
- Quick and easy frequency adjustment
- Single crystal easily generates multiple clocks
- Faster state machine utilizing different clock phases
  - Excellent for advanced memory types
- De-skew incoming clock
- Generate fast setup and hold time or fast clock-to-outs
DLL: Clock Mirrors

- **Input clock duplication**
  - Provides on and off-chip clocks
  - Clock distribution across system
- **Cleans and reconditions backplane or noisy clocks**
- **Extremely low output skew**
Spartan-IIE DLL Example
1X Clock Mirror with 180° Output Phase (100MHz)

Xilinx FPGA

1X

180

DLL

100 MHz Clock

100 MHz
(0 Phase)

100 MHz
(180 Phase)

Benefit - DDR Memory Interface - Avoid external DLLs
DLL: Multiplication

- Use 1 DLL for 2x multiplication
- Combine 2 DLLs for 4x multiplication
- Reduce board EMI
  - Route low-frequency clock externally and multiply clock on-chip
DLL: Multiplication Example

- Reduce EMI by increasing data width and decreasing clock frequency
- Cross over clock domains without worries
  - Synchronized clock edges
  - No external drift
  - Minimal external clock skew
DLL: 2x Multiplication Implementation

- Requires one CLKDLL primitive
- CLK0 output removes skew between registers on the chip
- CLK2X is 2X clock output
DLL: Division

- Selectable division values
  - 1.5, 2, 2.5, 3, 4, 5, 8, or 16
- Cascade DLLs to combine functions
- 50/50 duty cycle correction available
DLL: Phase Shift

- Phase shifts
  - 0°, 90°, 180°, and 270°
- Increase system performance by utilizing additional clock phases
- 50/50 duty cycle correction available
- Excellent for external memory interfaces
  - DDR and QDR RAM
DLL: Speedup Tsu/h and Tco

- Nullify clock line delay
  - External clock pin and internal clock are aligned
- Optional duty cycle correction
  - 50/50 duty cycle correction applied when specified
- Low sensitivity to clock input noise
  - Lower-cost oscillator

* Spartan-IIE data sheet module 3 Pin-to-Pin Parameters, LVTTL, 12 mA, Fast Slew Rate
Spartan-IIIE DLL Example
Clock-to-Out Improvement Using DLLs

Output standard = SSTL-3 Class-II
(OBUF_SSTL3_II)
Temp=100C, Vdd=2.375V, Vcco=3.3V, Vtt=1.5V

Waveforms:
1: CLkin
2: DATA OUT (no DLL)
3: DATA OUT (DLL deskewed)

Timing:

- w/o DLL - w/ DLL
- r->r - r->f - r->r - r->f
- 3.5n - 3.8n - 1.1n - 1.3n

Benefit - Increases Timing Budget - Allows Use of Cheaper Memories
System Clock Management Summary

• All digital DLL Implementation
  – Input noise rejection
  – 50/50 duty cycle correction
• Clock mirror provides system clock distribution
• Multiply input clock by 2x or 4x
• Divide clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16
• Provides 0, 90, 180, and 270 clock phase shift
• De-skew clock for fast setup, hold, or clock-to-out times
Spartan-IIIE Features

System Interfaces
Comprehensive I/O Connectivity

- Single ended and differential
  - Up to 514 single-ended, 205 differential pairs
  - 400 Mb/sec LVDS: ideal for Consumer Applications
  - 19 I/O standards, 8 flexible I/O banks
  - PCI 32/33 and 64/66 support

- Multiple package options

- 3 IOB registers: in, out, 3-state

- Voltages: 3.3V, 2.5V, 1.8V, 1.5V

Chip-to-Chip Interfacing:
- LVDS
- LVPECL
- LVC莫斯
- LVTTL

Backplane Interfacing:
- AGP
- GTL
- GTL+
- PCI
- BLVDS

High-speed Memory Interfacing:
- CTT
- HSTL
- SSTL
Basic I/O Block Structure

Three-State
FF Enable
Clock
Set/Reset
Output
FF Enable
Direct Input
FF Enable
Registered Input

Three-State Control
Output Path
Input Path

For Academic Use Only
Programmable Output Driver

- Significant EMI reduction benefit
- Programmable driver strength
  - Pull-up and Pull-down drivers can be individually controlled
  - 16 different setting for each
  - 2 slew rate settings

<table>
<thead>
<tr>
<th>Simultaneous Switching Output Guidelines</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
</tr>
<tr>
<td>BGA</td>
</tr>
<tr>
<td>LVTTL Slow Slew Rate, 2mA drive</td>
</tr>
<tr>
<td>LVTTL Slow Slew Rate, 4mA drive</td>
</tr>
<tr>
<td>LVTTL Slow Slew Rate, 6mA drive</td>
</tr>
<tr>
<td>LVTTL Slow Slew Rate, 8mA drive</td>
</tr>
<tr>
<td>LVTTL Slow Slew Rate, 12mA drive</td>
</tr>
<tr>
<td>LVTTL Slow Slew Rate, 16mA drive</td>
</tr>
<tr>
<td>LVTTL Slow Slew Rate, 24mA drive</td>
</tr>
<tr>
<td>LVTTL Fast Slew Rate, 2mA drive</td>
</tr>
<tr>
<td>LVTTL Fast Slew Rate, 4mA drive</td>
</tr>
<tr>
<td>LVTTL Fast Slew Rate, 6mA drive</td>
</tr>
<tr>
<td>LVTTL Fast Slew Rate, 8mA drive</td>
</tr>
<tr>
<td>LVTTL Fast Slew Rate, 12mA drive</td>
</tr>
<tr>
<td>LVTTL Fast Slew Rate, 16mA drive</td>
</tr>
<tr>
<td>LVTTL Fast Slew Rate, 24mA drive</td>
</tr>
<tr>
<td>LVCMOS2</td>
</tr>
<tr>
<td>PCI</td>
</tr>
<tr>
<td>GTL</td>
</tr>
<tr>
<td>GTL+</td>
</tr>
<tr>
<td>HSTL Class I</td>
</tr>
<tr>
<td>HSTL Class III</td>
</tr>
<tr>
<td>HSTL Class IV</td>
</tr>
<tr>
<td>SSTL2 Class I</td>
</tr>
<tr>
<td>SSTL2 Class II</td>
</tr>
<tr>
<td>SSTL3 Class I</td>
</tr>
<tr>
<td>SSTL3 Class II</td>
</tr>
<tr>
<td>CTT</td>
</tr>
<tr>
<td>AGP</td>
</tr>
</tbody>
</table>
Post-PCB Signal Integrity Adjustment
Optimizing Performance “As Built”

Initial Design: LVTTL_F16 (Fast slew, 16 mA)
Driver impedance too low – **Undershoot!**

Final Design: LVTTL_F8 (Fast slew, 8 mA)
Driver impedance ~50Ω – **No Undershoot**

Requires a Bitstream Change Only!
System Interfaces -- SelectI/O™

Voltage Standards
- 3.3V
- 2.5V
- 1.8V
- 1.5V

Chip-to-Chip Interfaces
- LVDS
- LVPECL
- LVCMOS
- LVTTL

Backplane Interfaces
- AGP
- GTL
- GTL+
- PCI
- BLVDS

High-speed Memory Interfaces
- CTT
- HSTL
- SSTL

- Supports multiple voltage and signal standards simultaneously
- Eliminate costly bus transceivers

For Academic Use OnlyFor Academic Use Only
## SelectI/O™ Standards

<table>
<thead>
<tr>
<th>Standard</th>
<th>$V_{REF}$</th>
<th>$V_{CCO}$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Chip to Chip Interface</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVTTL</td>
<td>na</td>
<td>3.3</td>
</tr>
<tr>
<td>LVCMOS2</td>
<td>na</td>
<td>2.5</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>na</td>
<td>1.8</td>
</tr>
<tr>
<td>LVDS</td>
<td>na</td>
<td>2.5</td>
</tr>
<tr>
<td>LVPECL</td>
<td>na</td>
<td>3.3</td>
</tr>
<tr>
<td><strong>Backplane Interface</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCI 33MHz 3.3V</td>
<td>na</td>
<td>3.3</td>
</tr>
<tr>
<td>PCI 66MHz 3.3V</td>
<td>na</td>
<td>3.3</td>
</tr>
<tr>
<td>GTL</td>
<td>0.80</td>
<td>na</td>
</tr>
<tr>
<td>GTL+</td>
<td>1.00</td>
<td>na</td>
</tr>
<tr>
<td>AGP-2X</td>
<td>1.32</td>
<td>3.3</td>
</tr>
<tr>
<td>Bus LVDS</td>
<td>na</td>
<td>2.5</td>
</tr>
<tr>
<td><strong>Memory Interface</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HSTL-I</td>
<td>0.75</td>
<td>1.5</td>
</tr>
<tr>
<td>HSTL-III &amp; IV</td>
<td>0.90</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL3-I &amp; II</td>
<td>1.50</td>
<td>3.3</td>
</tr>
<tr>
<td>SSTL2-I &amp; II</td>
<td>1.25</td>
<td>2.5</td>
</tr>
<tr>
<td>CTT</td>
<td>1.50</td>
<td>3.3</td>
</tr>
</tbody>
</table>

$V_{CCO}$ defines output voltage

$V_{REF}$ defines input threshold reference voltage

Available as user I/O when using internal reference
I/Os Separated into 8 Banks

Bank 0

Bank 1

Bank 2

Bank 3

Bank 4

Bank 5

Bank 6

Bank 7

IOB=I/O Blocks

GCLK0

GCLK1

GCLK2

GCLK3

For Academic Use Only
I/O Signal Types

- Single-Ended
  - LVCMOS
  - HSTL
  - SSTL
  - LVTTL

- Differential
  - LVDS
  - Bus LVDS
  - LVPECL

NOTE: Only the popular IO types shown here
Single Ended I/O

- Traditional means of data transfer
- Data is carried on a single line
- Bigger voltage swing between logic Low and High

![Diagram of single ended data transfer](image)

LVTTL input levels:
- Logic High: 3.3 V
- Logic Low: 0.8 V
- 1.2 V swing
# System I/O

## Single-Ended I/O Standards Summary

<table>
<thead>
<tr>
<th>Type</th>
<th>Chip to chip</th>
<th>Chip to Backplane</th>
<th>Chip to Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Key Standards</strong></td>
<td>LVTTL, LVC莫斯</td>
<td>GTL, GTL+, AGP</td>
<td>HSTL I, III, IV</td>
</tr>
<tr>
<td><strong>Key Highlights</strong></td>
<td>Higher voltage swing</td>
<td>Low voltage swing</td>
<td>Low voltage swing, low power, low noise, 200-400MHz</td>
</tr>
<tr>
<td><strong>Primary Usage</strong></td>
<td>Legacy interface</td>
<td>Pentium CPU, backplanes</td>
<td>High speed SRAM, MIPS/ UltraSparc-II</td>
</tr>
<tr>
<td><strong>Applications</strong></td>
<td>Glue logic, ASIC chip to chip</td>
<td>Datacom, Pentium, add-in cards</td>
<td>3-D graphics cards, plasma LCD displays, DTV interfaces, Set-Top Boxes</td>
</tr>
<tr>
<td><strong>Vendors</strong></td>
<td>Most vendors</td>
<td>Intel, TI</td>
<td>Micron, IDT, Cypress, MIPS, IBM, etc.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Micron, Samsung, Toshiba, Hyundai, NEC, Siemens, etc.</td>
</tr>
</tbody>
</table>
Differential I/O

- Latest means of data transfer
- One data bit is carried through two signal lines
  - Voltage difference determines logic High or Low
- Smaller voltage swing between logic Low and High
  - Higher performance
  - Lower power
  - Lower noise

LVDS Input levels
Select I/O: Differential I/O Types

- LVDS (Low Voltage Differential Signal)
  - Unidirectional data transfer

- Bus LVDS
  - Bi-directional communication between 2 or more devices
  - Can transmit and receive LVDS signals through the same pins

- LVPECL (Low Voltage Positive Emitter Coupled Logic)
  - Unidirectional data transfer
  - Popular industry standard for fast clocking
More Differential I/O Information

- Xilinx web site
  (http://www.xilinx.com/apps/xapp.htm)
  - Application Notes
    - XAPP230, XAPP231, XAPP232, XAPP233,
    - XAPP237, XAPP238, XAPP243, XAPP245

- National Semi. web site
  (http://www.national.com/appinfo/lvds)
  - LVDS Design Guide
  - BLVDS White Paper
System Interface Summary

• SelectI/O™ supports 19 IEEE/JEDEC I/O standards
  – High speed with differential I/Os
    • Low power, less noise
  – External high speed memory interface
    • Use HSTL and SSTL standards
  – High performance backplane applications
    • Use PCI, GTL and GTL+ standards

• Flexible I/O block
  – Programmable slew rate for EMI and ground bounce control
  – Independent input, output and programmable 3-state registers
  – Input delay for 0 hold time
Configuration Basics

- Spartan-IIIE device
  - Is SRAM-based and hence volatile
    - Needs a configuration data source
    - Needs to be re-configured (re-programmed) upon power-up
  - ISP
    - Re-programmable/upgradable in the field

- Configuration
  - Programming the device with design logic
Configuration

• Configuration data source
  – PROM
    • Serial/Parallel PROMs
  – Hard disk
  – Microprocessor memory

• Configuration interface
  – Simple serial
  – High-speed parallel
  – JTAG or boundary scan
  – IRL
  – Microprocessor
  – CPLD
JTAG Basics

- Also known as
  - IEEE/ANSI standard 1149.1
  - Boundary scan
- Set of design rules that facilitate
  - Testing
  - Programming
  - Debug
- Can be done at the chip, board, and systems level
- Can also have user-defined instructions
  - Example: vendor-specific instructions: configure and verify
JTAG Basics (cont’d)

• Rapid and automatic detection and isolation of defects due to common failures
  – Detect opens and shorts
• Ensure all components on PCB are
  – Mounted properly
  – In right place
  – Have proper interconnects among them
• Allows complete control and access to the boundary pins of a device without the need for
  – Bed-of-nails
  – Other test equipment
JTAG Compliant Device

- Includes a boundary-scan cell connected to each input, output or bi-directional pin
  - Transparent and inactive under normal conditions
- Test mode
  - Input signals captured and output signals set to affect other devices on the board
JTAG Mode

- Supports readback through boundary scan port
- Can mix any Xilinx device (FPGA, CPLD, PROM) and non-Xilinx devices in the chain
JTAG Mode (Cont’d)

• Dedicated TDI, TCK, TDO and TMS pins must operate at LVTTL
  – $V_{CCO}$ for bank 2 must be at 3.3V
• Maximum configuration rate of 33 MHz
Xilinx Web: Configuration Solutions
Xilinx Download Cables

• Types
  – MultiLINX™ cable
  – Parallel cable

• Perfect source for prototype and debugging

• Supports all traditional and JTAG-based configuration methods
Cable Software Support

• iMPACT software
  – Included in Xilinx Alliance and Foundation ISE software tools
Summary

- System Clock Management
- Embedded Memory
- System Interfaces
- Logic & Routing
- Configuration
Spartan-IIIE: A System-Level Solution

- Hierarchical memory support
  - SelectRAM+ can be used to create bytes or Kbytes of internal storage and access megabytes of fast external memory
- System speedup and synchronization
  - Nullify clock distribution delays - 160 MHz system performance
  - Synthesize clocks for internal and external use
  - Synchronize systems: create clock mirrors/nullify board delay
- System level integration
  - Connect directly to existing and emerging I/O standards
- Vector-based interconnect
  - Much more predictable before place and route
  - Enhances synthesis-based flows
Spartan-IIIE: A System-Level Solution

- IP solutions
- Software
  - Based on proven timing-driven place and route technology
- System-level features
  - RAM, DLLs, I/O standards
- Re-programmable
Reference Slides
SelectI/O™

• I/O can be programmed for 19 signal standards
  – Provides industry-standard IEEE/JEDEC I/O standards
  – Single-ended and differential
• Allows connection to
  – Processors, memory, bus-specific standards, mixed signal
  – High-performance backplanes
• Improved power and grounds ratio to minimize ground bounce
• Simple entry of I/O standards in design tools
Chip-to-Chip Interface Standards

ETL Enhanced transceiver logic
Chip-to-Chip Interface Standards (Cont’d)
Backplane Interface Standards

Bus LVDS

PCI

AGP-2X

GTL

GTL+
Memory Interface Standards

HSTL

SSTL3/2

CTT

For Academic Use Only
Select I/O Input Bank Rules

- Each bank has a single input reference voltage ($V_{\text{REF}}$)
  - Shared among all I/Os in the bank
  - All I/O types in a bank must use the same reference voltage
  - All $V_{\text{REF}}$ pins in a bank must be tied to the same voltage
- Inputs not requiring a $V_{\text{REF}}$ fit in the bank
  - LVTTL, LVCMOS, LVPECL, LVDS, PCI
- $V_{\text{REF}}$ pins in a bank available as additional I/O, iff ...
  - I/O type does not require $V_{\text{REF}}$
  - Otherwise, all $V_{\text{REF}}$ pins must be used to supply reference voltage
- OBUFTs with Keepers require a reference voltage and are treated as IOBUFs
- Input buffers with LVTTL, LVCMOS2/18, PCI33/66 supplied by $V_{\text{CCO}}$
Select I/O Output Banks

- Each bank has a single source voltage ($V_{CCO}$)
  - Shared among all I/Os in that bank
  - All I/O types in a bank must use the same voltage source
  - All $V_{CCO}$ pins in a bank must be tied to the same voltage
- Only one $V_{CCO}$ voltage for smaller pin count packages
  - TQ144, PQ208
- Outputs not requiring $V_{CCO}$ fit in the bank
  - GTL, GTL+
- Configuration pins need special consideration
  - Configuration pins are located on the right side of device in Banks 2 and 3
  - $V_{CCO}$ must be 3.3 volts for serial PROMs configuration
Single-Ended I/O Standards

Benefits

• Reduced EMI compared to 3.3V TTL
  – Low Output Voltage Swing
  – Slow Edge Rates (dV/dt)
• Reduced Power Consumption
• Reduced Noise With External Termination
  – Reduced reflection
  – Ringing
  – Cross-talk
• Higher Performance/Higher Bandwidth
Differential I/O Benefits

**I/O Connectivity**

- Significant Cost Savings
  - Reduced EMI
  - Fewer pins
  - Fewer PCB layers, fewer PCB traces (PCB area savings)
  - Fewer/smaller connectors
  - No external transceivers
- High performance per pin pair - up to 400 Mb/sec
- Reduced EMI due to low output voltage swing
- High noise immunity
- Reduced power consumption
- Spartan-IIIE Supports LVDS, Bus LVDS, and LVPECL
Select I/O: Differential I/O

- Differential I/O is a standard feature
  - Supported in all devices densities, all speed grades
- More differential I/Os within a device
  - Up to 240 I/O pairs
  - Offers flexibility in board layout
- Flexible differential I/Os
  - Use any I/O as input, output or bi-directional
- Spartan-IIIE
  - Can be driven by any standard LVDS/LVPECL driver
  - Complies with LVDS/LVPECL receiver specs
Select I/O: Differential I/O Configurations

- **Point to Point**
  - One transmitter and one receiver
  - Mostly used by LVDS/LVPECL in chip-to-chip applications

- **Multi-Drop**
  - One transmitter and multiple receivers
  - Used by Bus LVDS/LVPECL in backplane applications

- **Multi-point**
  - Multiple transceivers
  - Used by Bus LVDS/LVPECL in backplane applications
Select I/O: LVDS & LVPECL

- All I/Os have LVDS/LVPECL capability
- Differential signal pairs can be used as
  - Synchronous inputs or outputs
  - Asynchronous inputs
  - Some as asynchronous outputs
- Synchronous
  - Signal comes from IOB flip-flop
- Asynchronous
  - Signal comes from internal logic
What is LVDS?

• LVDS - Low Voltage Differential Signaling
• LVDS is a differential signaling interconnect technology
  – Requires two pins per channel
• LVDS was first used as a interconnectivity technology in
  laptops and displays to alleviate EMI issues
• Technology is now widely used
  – A broad spectrum of telecom and networking applications
  – Mainstream consumer applications like digital video and
    displays
LVDS Benefits

• Higher I/O speed
• Lower cost
  – Serialize multiple single-ended to differential channel signals
  – Save I/O pins
  – Use a smaller package
  – Save board space
• Technology and process independent
  – Easy migration path for lower supply voltages
  – Maintain same signal levels
  – Maintain same performance
• Low power
• Low noise
• Low EMI
LVDS Low Power Advantage

• LVDS technology saves power in several important ways
• Power dissipation at the terminator is \(~1.2\) mW
  – RS-422 driver delivers 3 V across a termination of 100 \(\Omega\), for 90 mW power consumption... 75 times more than LVDS!
• Due to the current mode driver design, the frequency component of ICC is greatly reduced
  – Compared to TTL/CMOS transceivers where the dynamic power consumption increases exponentially with frequency
LVDS Noise Immunity Advantage

- $R_{\text{OUT}}$ is clean even in cases of extreme common mode noise contamination
LVDS benefits - Low EMI

- Low voltage swing (~350mV)
- Slow edge rates compared to other technologies (1V/ns)
- Current mode of operation ensures low $I_{CC}$ spikes
- High noise immunity
  - Switching noise cancels between the two lines
  - Data is not effected by the noise
    - External noise effects both lines, but the voltage difference stays about the same
LVDS Applications

• Communications and Networking
  – Switches
  – Repeaters
  – Wireless base stations

• Data Communications
  – Routers
  – Hubs
LVDS Applications (cont’d)

• Consumer Electronics
  – Digital cameras
  – Flat panel displays

• Office/Home
  – Printers
  – Copiers

• Various backplane applications
Spartan-IIIE LVDS Benefits

• Exceptional performance
  – Up to 400Mb/sec. per differential pair

• Significant Cost Savings
  – Reduced EMI
  – Fewer pins (smaller package)
  – Fewer PCB layers
  – Fewer PCB traces (PCB area savings)
  – Fewer/smaller connectors
  – No transceivers

• Quicker Time-to-market
  – Fewer EMI issues
LVDS Driver and Receiver

Driver

Spartan-IIE FPGA

2.5V

DATA Transmit

LVDS Output

$V_{CCQ} = 2.5V$

$Z_0 = 50\Omega$

to LVDS Receiver

$R_S = 165$

$R_{DIV} = 140$

1/4 of Bourns Part Number CAT16-LV4F12

Receiver

from LVDS Driver

$Z_0 = 50\Omega$

LVDS IN

$R_T = 100\Omega$

LVDS IN

Spartan-IIE FPGA

DATA Receive
Select I/O: Bus LVDS

- All I/Os have Bus LVDS capability
- Fully compatible with industry-standard Bus LVDS devices from National Semiconductor and other vendors
LVDS Benefits – Reduced I/O Count

Example

Single-ended I/O

LVDS I/O

# of Pins: 80

# of Pins: 46
Spartan-IIE LVDS Example

Clock Distribution

Clock speeds of 200 MHz+ can be distributed with ease using LVDS
Spartan-IIE Eliminates LVDS-to-TTL Converters -- Eliminates 2ns Delay & Skew

Benefits - Higher performance, low EMI, lower cost, fewer components
Spartan-IIIE LVDS Example
Clock Conversion with Zero Delay

Zero-Delay Local Clock Generation to Any of Spartan-IIIE I/O Standards

Benefits - Low EMI, lower cost, fewer components
LVPECL Benefits

• Higher I/O speed
• Board-level clock distribution
  – Zero-delay conversion of LVPECL clocks into virtually any other I/O standard
• Lower cost
  – Serialize multiple single-ended to differential channel signals
  – Save I/O pins
  – Use a smaller package
  – Save board space
• Low power
• Low noise
• Low EMI
LVPECL Applications

• Backplanes
• High performance clocking
  – 100 MHz and above
• Optical Transceiver
• High speed networking
• Mixed-signal interfacing
LVPECL Driver and Receiver

Driver

Spartan-IIIE FPGA

3.3V

DATA Transmit

1/4 of Bourns Part Number CAT16-PC4F12

$R_o = 100$

Z0 = 50Ω

LVPECL_OUT

to LVPECL Receiver

Receiver

from LVPECL Driver

$Z0 = 50Ω$

LVPECL_IN

Spartan-IIIE FPGA

$R_T = 100Ω$

DATA Receive
LVPECL: Clock Conversion

- Receive and convert high speed clocks with zero delay
- Zero-delay clock generation to any of SelectI/O Standards
- Eliminate costly bus translators
Configuration Methods

- Master serial mode
- Slave serial mode
- Slave parallel mode
- JTAG mode
- IRL

- Multiple devices can be daisy-chained in
  - Master serial mode
  - Slave serial mode
  - JTAG mode
Master Serial Mode

- Spartan-IIE device acts like a master
  - Generates configuration clock (CCLK) using internal oscillator
- PROM stores the configuration data
- Configuration rate selectable from 4-60 MHz
  - -30% to +45% variance due to process dependence
Slave Serial Mode

- Spartan-IIE device acts like a slave
  - An external clock source drives the CCLK pin
- Configuration data is stored in PROM, flash, microcontroller or microprocessor memory
- Maximum configuration rate of 66 MHz
Slave Parallel Mode

Single or multiple Spartan-IIE devices connected in parallel
Slave Parallel Mode (cont’d)

• Spartan-IIIE device acts like a slave
  – An external clock source drives the CCLK pin
  – Microprocessor, Microcontroller or CPLD controls configuration

• Configuration data is stored in parallel PROM, flash, Microcontroller or Microprocessor memory

• Fastest configuration mode
  – 8 bits per CCLK cycle
  – 50MHz configuration rate (400 Mbit/sec)

• Supports Readback
  – Bi-directional read/write port for configuration and readback
• Internet Reconfigurable Logic (IRL)
  – IRL is a design methodology to create field upgradable applications
  – Supported by products, design guidelines and reference designs

• Xilinx Online
  – Xilinx program to enable, identify and promote field upgradable applications
IRL Methodology Elements

• 4 main elements in IRL model
  – Host / Server
  – Network
  – Target to be updated
  – Payload(s)
• Xilinx provides an API (PAVE) and a set of design guidelines that define how remote devices can be upgraded via a network.
PAVE Features

• Configures FPGAs / CPLDs
  – IEEE 1149.1 JTAG / SelectMAP
• PAVE Payload upgrades PLD + system software
• Systems Integration Framework (SIF) within Wind River’s Tornado® environment
• PAVE source distributed and supported by Xilinx
MultiLINX™ Cable

- Configuration and Readback support
  - Using boundary scan (JTAG) mode
  - Slave serial/parallel mode
- Supports USB interface on PC
  - Fastest configuration
  - Baud rate up to 12M
- Supports RS-232 interface on PC and UNIX
  - Baud rate
    - Up to 57.6K on PC
    - Up to 38.4K on UNIX

For Academic Use Only
For Academic Use Only
Parallel Cable

- Configuration and Readback support
  - Using boundary scan (JTAG) mode
- Supports parallel port on PC
  - Baud rate up to 57.6K
Parallel Cable

Top View

Bottom View

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