1) Design a BCD to Decimal decoder.

2) Design a BCD to Seven Segment decoder circuit for displaying decimal digits.

3) Design a combinational circuit that converts a decimal digit from the 2,4,2, 1 code to 8,4, -2, -1 code.

4) Design a module-8 counter which counts in the way specified below. (use JK FF's)

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Gray Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>1</td>
<td>001</td>
</tr>
<tr>
<td>2</td>
<td>011</td>
</tr>
<tr>
<td>3</td>
<td>010</td>
</tr>
<tr>
<td>4</td>
<td>110</td>
</tr>
<tr>
<td>5</td>
<td>111</td>
</tr>
<tr>
<td>6</td>
<td>101</td>
</tr>
<tr>
<td>7</td>
<td>100</td>
</tr>
</tbody>
</table>

5) Analyze the synchronous circuit below (clock is not shown but it is implicit).
   a) Write down the excitation and output function.
   b) Form the excitation and state tables.
   c) Give a word description of the circuit operation.
6) Determine the P.I.’s of the function:
\[ F(A, B, C, D) = \sum (1, 4, 6, 7, 8, 9, 10, 11, 15) \]

7) Determine the output F1, F2, and F in the circuits shown below:

8) Draw the logic diagram of an Exclusive-OR by using NAND gates.

9) Obtain the simplified expressions in S.O.P. for the following functions:

a) \[ ABD + \overline{ACD} + \overline{AB} + \overline{ACD} + \overline{ABD} \]

b) \[ \overline{XZ} + \overline{WXY} + W(\overline{XY} + X\overline{Y}) \]

c) \[ \overline{AC} + \overline{BC} + \overline{BC} + ABC \]
10) Design a counter with the following binary sequence:

0, 1, 3, 2, 6, 4, 5, 7 and repeat (use RS FF’s)

11) Derive the state table and state diagram of the sequential circuit below. What does the circuit do?

12) A sequential circuit has two flip-flops (A and B), two Inputs (x and y) and an output (Z). The flip-flop input functions and the circuit output functions are as follows:

\[ J_A = X'B + Y'B' \quad K_A = XY'B' \]
\[ J_B = XA' \quad K_B = XY' + A \]
\[ Z = XYA + X'Y'B \]

Obtain the logic diagram, state table, state diagram and state equations of this sequential circuit.
13) A sequential circuit (SISO) has the following state diagram. Design this sequential circuit using T-FF’s. Repeat your design by using RS-FF’s.

![State Diagram](image)

14) A special flip-flop is to be designed. The description of this FF is given below:

\[ Q^{n+1} = Y \otimes Q^n \quad \text{if} \ x = 0 \]
\[ Q^{n+1} = Y \oplus Q^n \quad \text{if} \ x = 1 \]

Design this flip-flop using:
(a) Clocked RS flip-flop
(b) Clocked JK flip-flop.
15) Design a sequential function which will detect the sequence

"...11010..."

whenever it occurs. Draw the state diagram and state table.

16) Design the Full Adder/Subtractor shown below. There are four inputs (Ai, Bi, CBi and F) and two outputs (SD and CB0). The input F is a control signal such that when F=0 the circuit works as a full adder and:

- Ai and Bi represent the two bits to be added,
- CBi presents the input carry,
- SD presents the output sum, and
- SB0 presents the output carry.

When F=1 the circuit works as a full subtractor and:

- Ai and Bi represents the two binary bits to be subtracted,
- CBi represents the input borrow,
- SD represents the output difference, and
- CB0 represents the output borrow.

Implement the circuit using the minimum number of gates.
17) The schematic diagram shown in Figure 2 shows a ternary full adder that receives two ternary digits X and Y plus a carry-in Ci and produces the sum S in base 3 plus a carry-out Co. The ternary digits are coded by two binary digits: 0 by 00, 1 by 01, and 2 by 10. Thus, for example, if X and Y are each equal to 2 in base 3 and Ci equals 1, the ternary full adder is required to perform the ternary addition of $(2)_3 + (2)_3 + (1)_3 = (12)_3$. Accordingly, the sum S must be 2 while the carry-out must be one. Design the circuit assuming you have as many gates as necessary as well as binary half and full adders.