ECE 526

Digital Design with Verilog and SystemVerilog

Catalog Course Description

ECE526 Digital Design with Verilog and SystemVerilog

Prerequisite: ECE 320/L. Corequisite: ECE 526L. This course covers the use of Verilog and SystemVerilog Languages (IEEE Std. 1800) for the design and development of digital integrated circuits, including mask-programmed integrated circuits (ASICs) and field programmable devices (FPGAs). Hierarchical top down vs. bottom up design, synthesizable vs. non-synthesizable code, design scalability and reuse, verification, hardware modeling, simulation system tasks, compiler directives and subroutines are all covered and illustrated with design examples.

Instructor

• Dr. Ronald W. Mehler
• Jacaranda 3303
• Office Hours: TBD

Prerequisite

ECE 320: Theory of Digital Systems

Boolean algebra, combinational and sequential circuits, number systems, etc.

Advised:

At least two 400-level computer engineering courses such as 420, 422, 425 and 442.

Neither ECE526 nor any other 500-level course is a beginner’s course.

Books


Warning: text covers only Verilog. We will be mixing in SystemVerilog too.

Interesting Reading:


Course Web Page

http://www.csun.edu/~rmehler/526f19.html
Lab Manual

- Digital Design with Verilog and SystemVerilog Laboratory
- Posted on course web site
  - May be modified during the semester
  - Only use the course web site, not any other CSUN site that may have old versions.

Lab Access

- To use the lab, you will need a user ID and password.
- If you are registered, you should have one of each.
- If you don’t know what yours are, see the web site
  - [http://www.csun.edu/it/helpdesk/outages/accounts.html](http://www.csun.edu/it/helpdesk/outages/accounts.html)

Login Problems

Would recommend that all students be asked to reset their password at the beginning of the semester so that their account info are current and updated. Also, please note that if the student does not know their password, we (Information Systems) will not be able to reset it. They would have to go over to the Campus Helpdesk Walk-In Center - located in Oviatt Library, room 32 (Garden Level). The Center is open from Mon-Thu 8 a.m. to 7 p.m., and on Fri. 8 a.m. to 5 p.m. Picture ID is required for password resets.

Please note that if the student has never been able to login successfully to a Windows machine in the CECS labs that most likely be/she has never reset their CSUN password. The password can be reset through the Campus Portal, under the Technology Tab.

Linux Computer Access

- Computers in this room are almost the only ones on campus that run the required software.
  - Two or three in Sr. Design lab should work too
- This room is only open during lab hours.
- You can access these machines remotely from the common lab.
- You can also use your own computers to remotely log in from anywhere.

Remote Access

- Need VPN and X windowing programs
- Download VPN from university
- Numerous X Windows programs are available, some free, some not
  - Xming (requires font installation too)
  - MobaXterm
  - Xshell
  - Xmanager
  - Windows 10 Bash shell

Common Lab (JD 1622C) Hours

<table>
<thead>
<tr>
<th>Day</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mon</td>
<td>8 a.m. – 11 p.m.</td>
</tr>
<tr>
<td>Tue</td>
<td>8 a.m. – 11 p.m.</td>
</tr>
<tr>
<td>Wed</td>
<td>8 a.m. – 11 p.m.</td>
</tr>
<tr>
<td>Thu</td>
<td>8 a.m. – 11 p.m.</td>
</tr>
<tr>
<td>Fri</td>
<td>8 a.m. – 6 p.m.</td>
</tr>
<tr>
<td>Sat</td>
<td>8 a.m. – 6 p.m.</td>
</tr>
<tr>
<td>Sun</td>
<td>8 a.m. – 6 p.m.</td>
</tr>
</tbody>
</table>
COURSE POLICY

1. Homework and laboratory exercises will be assigned. They will be collected on due dates. Keep a copy of all solutions because homework solutions might not be returned. **No late homework will be accepted.**

2. Three exams will be given (two midterm exams and one final exam). Tentative dates of the midterm exams are lab days in the 7th and 12th week of classes. There will be no lab on exam days.

3. Exam solution should be in Blue Books. (These can be bought at the bookstore.) **Absolutely no other solution papers will be accepted.** The Blue Books will be collected at the beginning of the semester and returned back on the exam day.

4. Exams are cumulative; study everything for every exam.

5. **Absolutely no make-ups** on exams. For emergency, you will be allowed to miss only one midterm exam with no penalty. The final exam **must** be taken to pass the course.

6. The weights of the exams and exercises will be as follows:

<table>
<thead>
<tr>
<th>Exam</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>30%</td>
</tr>
<tr>
<td>#2</td>
<td>30%</td>
</tr>
<tr>
<td>Final</td>
<td>35%</td>
</tr>
<tr>
<td>Total</td>
<td>95%</td>
</tr>
</tbody>
</table>

7. The remaining 5% will be given on homework as well as the general impression given by each student. Talking to neighbors or coming late to the class disturbs the class and gives a bad impression. Please avoid doing that and participate in classroom discussions to guarantee a big portion of the 5%.

8. Your final grade will directly reflect the total number of points you will get. The following are the percentages for each grade:

<table>
<thead>
<tr>
<th>Grade</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>90-100%</td>
</tr>
<tr>
<td>A-</td>
<td>85-89%</td>
</tr>
<tr>
<td>B+</td>
<td>82-84%</td>
</tr>
<tr>
<td>B</td>
<td>78-81%</td>
</tr>
<tr>
<td>B-</td>
<td>75-77%</td>
</tr>
<tr>
<td>C+</td>
<td>72-74%</td>
</tr>
<tr>
<td>C</td>
<td>68-71%</td>
</tr>
<tr>
<td>C-</td>
<td>65-67%</td>
</tr>
<tr>
<td>D+</td>
<td>60-64%</td>
</tr>
<tr>
<td>D</td>
<td>55-59%</td>
</tr>
<tr>
<td>D-</td>
<td>50-54%</td>
</tr>
<tr>
<td>F</td>
<td>Below 50%</td>
</tr>
</tbody>
</table>

Course Policy

- ECE 526 and ECE 526L are separate courses.
- Courses are co-requisites. It is required to take both concurrently.
- ECE 526L grade will be solely the average of all lab reports.
- Lab reports will have no bearing on ECE 526 grade.

Academic Dishonesty

- Claiming credit for someone else’s work is the ultimate sin in academia.
- Your instructor is as hard core as they come on this.
- Not only will cheating result in an F in the course, it may result in expulsion from the university.
- International students found guilty of academic dishonesty may be deported.

It’s NOT a Victimless Crime

- Giving diplomas to engineers who don’t know engineering quickly damages the reputation of the university.
- A cheater prevents those who come after from even getting interviews.

Swine Flu

Class presentation materials will be made available on the course web site. If you are sick, stay home and don’t infect anyone else.
The only stupid question is one you don’t ask.

“Better to keep your mouth shut and be thought a fool than to open it and remove all doubt.” -- Mark Twain

What’s an ASIC, Anyhow?

• Application Specific Integrated Circuit
  – Processors are generally NOT considered ASIC though design methodology is essentially identical. Processors (including DSP’s) are multi-purpose devices.
• Pretty much all digital integrated circuits are developed using ASIC methodology.
• Many times more ASICs are designed every year than GP Processors or other catalog parts.

ASIC Classes

- Custom Mask
- FPGA
- Full Custom
- Standard Cell
- Gate Array
- Structured
- Unstructured

It’s a Hot Field

More every day: Monster search done Aug. 20.

Job Posting (Aug. 19)

TECHNICAL SKILLS:

Use software development tools for microcontrollers. Must have experience with verification test languages such as Vera, Specman, and their extensions. Must know VHDL or Verilog language and using synthesis tools. Must know how to do C-level and ASM level programming/debug. Must have basic understanding of electrical interfacing of microcontroller into system level environment.
Digital Design

- Virtually all digital design is now done in ASICs.
- Virtually all ASICs are designed using an HDL and logic synthesis.
- Verilog is the HDL of choice among most engineers and companies, particularly in California.
- A few use VHDL.

Karnaugh Map

```
0 1 1 1 0
1 1 1 0
1 0 0 1
0 0 0 1
```

Minimize Functions Manually

```
0 1 1 1 0
1 1 1 0
1 0 0 1
0 0 0 1
```

Translate to Gates

“Best” design may be smallest, fastest, lowest power, quickest to market. Any one design will not be best in all categories.

Redundancy For Reliability

The smallest design might not be the most desirable.

Four-bit Counter
Encode States (half table shown)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>Current State</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Manual Minimization Limits

- Anyone can make a K-map for 4 inputs.
- 5 inputs is a bit tedious, but still manageable. Beyond 6?
- Useful devices tend to have a lot of states and inputs.
- Sum of products may not be the best implementation.
- Consider something so basic as a stoplight controller—pretty simple compared to a Pentium-class processor.

Stoplight Controller

- States: Red, Yellow, Green for each direction.
- Left-turn arrows: maybe 4, maybe 8
- Right-turn arrows: maybe 4
- Pedestrian lights: several possible states
- Sensors: push buttons and magnetic detectors
- Emergency Services override
- Fail-safe mode
- Once a single controller is perfect, synchronize it with the rest of the city.

Moore’s Law

2005: “Cell” processor has 234 million transistors
2006: Intel produces 153 megabit SRAM with > 1 billion transistors
2007: “Peryn” dual-core has 410 million, quad-core will have 820

Engineering Density in the USA
EDA: Electronic Design Automation

The process of using computer-based software systems to design very large-scale integrated (VLSI) circuits.

All modern integrated circuits are designed with EDA tools.

This course uses Verilog/SystemVerilog for hardware description and Synopsys VCS for simulation.

Course Outline

1. Introduction to EDA (Electronic Design Automation).
2. Introduction to Hardware Modeling
3. Verilog primitive operators and structural modeling
4. Design verification: folded into other topics
5. Synchronization and synchronous design
6. Top down and bottom up methodology
7. Library modeling moved to 527

Homework

• Review ECE 320 material, prepare for assessment test
• Read Palnitkar through Chapter 2
• Read Lab Manual through Experiment 1
• Make sure you have access to your UNIX account
• No deliverables this week