After Studying Chapter 15, You Should Be Able to:

- Explain the differences between harmonic and relaxation oscillators.
- Analyze and explain the operation of the RC phase-shift and Wien bridge oscillators.
- Analyze and explain the operation of the JFET as a voltage-variable resistor (VVR) and apply it to stabilize the output amplitude of the Wien bridge oscillator.
- Explain and analyze the use of active negative feedback to provide a Wien bridge oscillator with an adjustable output frequency.
- Explain high-frequency harmonic oscillators and the role of series and parallel resonant circuits.
- Analyze and discuss the operation of the Colpitts, Clapp, and Hartley oscillators.
- Discuss the characteristics of the crystal.
- Analyze and explain the operation of the Pierce (and other) crystal oscillator circuits.
- Explain the operation of the unijunction transistor (UJT).
- Explain and analyze the UJT relaxation oscillator.
- Explain and analyze the op amp relaxation oscillator.
- Explain and analyze the op amp triangle waveform generator.
The Barkhausen criteria for sustained oscillation set forth two conditions. First, the feedback must be positive. This means that the feedback voltage (or current) must be phased so that it adds to the amplifier's input signal. Second, the loop gain must be larger than unity to allow oscillations to build up. and equal to unity to sustain them. All harmonic oscillators must satisfy the Barkhausen criteria.

Consequently, an audio-frequency range (20 to 20 kHz) harmonic (sinusoidal output) oscillator must contain three basic ingredients:

1. An amplifier
2. A frequency-determining network
3. Positive (regenerative) feedback

The amplifier provides the voltage gain required to sustain oscillation. The frequency-determining network is configured to provide positive feedback at one particular frequency (the desired frequency of oscillation).

In Section 15-4 we shall add a fourth requirement termed adaptive negative feedback. Adaptive-negative-feedback circuitry is typically designed to allow the amplifier circuit initially to have a sufficiently large voltage gain to allow the oscillations to build up. This means the loop gain will be greater than unity. Once the desired output signal level is reached, the adaptive negative feedback circuitry automatically reduces the gain of the amplifier system. This, in turn, reduces the loop gain to unity and ensures a low-distortion sinusoidal output waveform.

### 15-3 A Phase-Shift Oscillator

To provide positive feedback at one particular frequency, an inverting amplifier may be used with a feedback network that supplies 180° of phase shift at the desired frequency of oscillation ($f_o$ - see Fig. 15-1(a)). Alternatively, a noninverting amplifier may be used with a frequency-determining feedback network that offers 0° of phase shift at $f_o$ [see Fig. 15-1(b)]. The phase-shift oscillator implements the topology indicated in Fig. 15-1(a) [refer to Fig. 15-1(c)].

The equivalent circuit of the phase-shift oscillator has been indicated in Fig. 15-2(a). When the magnitude of the gain of the amplifier is $A_{v1}$, the gain (an attenuation) of the feedback network (β) can have a magnitude no less than $1/A_{v1}$ in order to maintain the oscillation. This will provide a loop gain of unity.

When a phase-shift network such as that indicated in Fig. 15-2(a) is employed in a phase-shift oscillator, the $R$'s and $C$'s must be selected so as to produce 180° of phase shift at the desired frequency of oscillation. The output of the voltage amplifier is directed into the input of the phase-shift network. Thus

$$V_1 = V_{out}$$

The output resistance of the amplifier is designed to be very small compared to the input impedance of the phase-shift network. This is not too difficult to achieve when an op amp is employed.

The output voltage of the phase-shift network ($V_2$) is fed into the input of the...
amplifier. The amplifier's input resistance must be much larger than the output impedance of the phase-shift network, or its loading effects must be included in the analysis. Initially, we shall assume that the former case exists. From Fig. 15-2(a),

\[ V_2 = V_m \]

Using the assumptions above, we arrive at the equivalent circuit given in Fig. 15-2(b).

A rigorous analysis of most oscillator circuits can be conducted by performing the following steps:

1. Derive an equation for the voltage gain (B) of the feedback network (e.g., \( V_2/V_1 \)).
2. Place the resulting equation in the form \( a + jb \). (If there are no imaginary terms in the numerator, additional algebraic steps can be avoided by stopping the algebraic manipulation when the denominator is in the form above.)

3. Set the imaginary term \((j\cdot term)\) equal to zero, and solve for \( f_0 \) (the frequency of oscillation).

4. Substitute the result above into the equation for \( \beta \) obtained in step 1, and determine the magnitude of \( \beta \) at \( f_0 \).

These steps will produce an equation to determine the frequency of oscillation, and also assist us in the determination of the minimum voltage gain required to ensure oscillation. Consider Fig. 15-2(b).

The applied voltage \( V_1 \) produces three mesh currents: \( I_1, I_2, \) and \( I_3 \). The output voltage of the network is \( V_2 \), where

\[
V_2 = I_3R
\]

To find the voltage gain \( \beta \) of the phase-shift network, we must solve for \( I_3 \) since...
\[ \beta = \frac{\text{output voltage of the feedback network}}{\text{input voltage of the feedback network}} = \frac{V_2}{V_1} \frac{l_3 R}{V_1} \]

The three mesh equations for the network can be written as indicated by

\[ -V_1 + \left(-j \frac{1}{\omega C}\right) I_1 + R(I_1 - I_2) = 0 \]  
(15-1)

\[ R(I_2 - I_1) + \left(-j \frac{1}{\omega C}\right) I_2 + R(I_2 - I_3) = 0 \]  
(15-2)

\[ R(I_3 - I_2) + \left(-j \frac{1}{\omega C}\right) I_3 + RI_3 = 0 \]  
(15-3)

To solve the set of mesh equations for \( I_3 \), we shall first place them in standard form and then apply Cramer's rule and determinants. The reader is encouraged to work through the development that follows.

\[ \left(R - j \frac{1}{\omega C}\right) I_1 - RI_3 + 0I_2 = V_1 \]  
(15-4)

\[ -RI_1 + \left(2R - j \frac{1}{\omega C}\right) I_2 - RI_3 = 0 \]  
(15-5)

\[ 0I_1 - RI_2 + \left(2R - j \frac{1}{\omega C}\right) I_3 = 0 \]  
(15-6)

Now, by Cramer's rule and determinants, we have

\[ I_3 = \frac{\begin{vmatrix} R - j/\omega C & -R & V_1 \\ -R & 2R - j/\omega C & 0 \\ 0 & -R & 0 \end{vmatrix}}{\begin{vmatrix} R - j/\omega C & -R & 0 \\ -R & 2R - j/\omega C & -R \\ 0 & -R & 2R - j/\omega C \end{vmatrix}} \]

The \( 3 \times 3 \) matrices can be reduced to \( 2 \times 2 \) matrices by using cofactors. (Do not let this technique hinder you if you are familiar with another.)

\[ I_3 = \begin{vmatrix} R - j/\omega C & 2R - j/\omega C \\ -R & 0 \end{vmatrix} \begin{vmatrix} -R & 0 \end{vmatrix} + [V_1] \begin{vmatrix} -R & 2R - j/\omega C \\ 0 & -R \end{vmatrix} \]

Tenacity, a bottle of aspirin, and algebraic manipulation lead us to the following result:

\[ I_3 = \frac{R^2 V_1}{\begin{vmatrix} R - j/\omega C \end{vmatrix} (2R - j/\omega C)^2 - R^2} + (R)(-R)(2R - j/\omega C) \]

\[ = \frac{\begin{vmatrix} R - j/\omega C \end{vmatrix} (4R^2 - j4R/\omega C - 1/\omega C)^2 - R^2} - (R^3)(2R - j/\omega C) \]

\[ = \frac{\begin{vmatrix} R - j/\omega C \end{vmatrix} (3R^2 - j4R/\omega C - 1/\omega C)^2} - 2R^3 + jR^2/\omega C \]
Our final equation for \( I_3 \) is given by

\[
I_3 = \frac{R^2 V_1}{R^3 - 5R/\omega^2 C^2 + j(1/\omega^2 C^3 - 6R^2/\omega C)}
\]  

(15-7)

Now since \( V_2 = I_3 R \), Eq. 15-7 provides us with the expression

\[
V_2 = \frac{R^3}{R^3 - 5R/\omega^2 C^2 + j(1/\omega^2 C^3 - 6R^2/\omega C)} V_1
\]

Dividing both sides by \( V_1 \) yields \( \beta \).

\[
\beta = \frac{V_2}{V_1} = \frac{R^3}{R^3 - 5R/\omega^2 C^2 + j(1/\omega^2 C^3 - 6R^2/\omega C)}
\]  

(15-8)

Dividing the numerator and the denominator by \( R^3 \) leads us to

\[
\beta = \frac{V_2}{V_1} = \frac{1}{(1 - 5/\omega^2 R^2 C^2) + j(1/\omega^2 R^2 C^3 - 6/\omega R C)}
\]  

(15-9)

In order for the feedback network to provide 180° of phase shift, the imaginary term must be equal to zero, and the real term must be negative at the desired frequency of oscillation (\( f_o \)). We shall first determine the frequency at which the imaginary term is equal to zero. Note that \( \omega_o \) is equal to 2\( \pi f_o \). Hence

\[
\frac{1}{\omega_o^2 R^2 C^3} - \frac{6}{\omega_o R C} = 0
\]

\[
\omega_o R C - 6\omega_o^3 R^2 C^3
\]

\[
(\omega_o R C)^3(\omega_o R C) = 0
\]

Multiplying both sides by the denominator yields

\[
\omega_o R C - 6\omega_o^3 R^2 C^3 = 0
\]

Dividing both sides by \( \omega_o R C \) produces

\[
1 - 6\omega_o^2 R^2 C^2 = 0
\]

\[
6\omega_o^2 R^2 C^2 = 1
\]

Solving for \( \omega_o \), we have

\[
\omega_o^2 = \frac{1}{6R^2 C^2}
\]

or

\[
\omega_o = \frac{1}{\sqrt{6} R C} \quad \text{and} \quad f_o = \frac{1}{2\pi \sqrt{6} R C}
\]

Therefore, at

\[
\omega_o = \frac{1}{\sqrt{6} R C}
\]

the feedback factor \( \beta \) is

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\[ \beta = \frac{V_2}{V_1} = \frac{1}{(1 - 5/\omega^2 R^2 C^2) + j(1/\omega R^2 C - 6/\omega R C)} \]

\[ = \frac{1}{1 - \left[ \frac{5}{\left( \frac{1}{\sqrt{6} RC} \right)^2 R^2 C^2} \right] + j0} = \frac{1}{1 - \left[ \frac{5}{\left( \frac{1}{6 R^2 C^2} \right) R^2 C^2} \right]} \]

\[ = \frac{1}{1 - 30} = -\frac{1}{29} \]

and for oscillation to occur the loop gain (\(\beta A_v\)) must be greater than or equal to unity. Thus for the \(RC\) phase-shift oscillator, we have the conditions given in

\[ f_o = \frac{1}{2\pi \sqrt{6 \, RC}} \]

\[ A_v \geq 29 / 180^\circ \] \hspace{1cm} (15-10)

where \(f_o\) is the \(RC\) phase-shift oscillator frequency of oscillation in hertz and \(A_v\) is the amplifier’s required voltage gain.

In Fig. 15-3 we see an op amp phase-shift oscillator. The op amp is being used in its inverting amplifier configuration. As we can see, at \(f_o\), the frequency-determining network provides 180° of phase shift. Since we have an inverting amplifier, the total phase shift around the loop is 360° (0°), and the feedback signal will be in phase with the input. Therefore, the feedback will be positive (or regenerative), and the circuit will oscillate.

**FIGURE 15-3** Op amp RC phase-shift oscillator.
EXAMPLE 15-1

Analyze the phase-shift oscillator given in Fig. 15-3. Determine if the voltage gain and input resistance of the amplifier is adequate. Also find the frequency of oscillation.

SOLUTION First, we determine the range of possible voltage gains. When the potentiometer is fully counterclockwise,

\[ A_v = \frac{R_2 + R_3}{R_1} = \frac{-910 \, \text{k\Omega} + 0 \, \Omega}{33 \, \text{k\Omega}} = -27.6 \]

When the potentiometer is fully clockwise, the voltage gain will be at its maximum.

\[ A_v = \frac{R_2 + R_3}{R_1} = \frac{-910 \, \text{k\Omega} + 200 \, \text{k\Omega}}{33 \, \text{k\Omega}} = -33.9 \]

Since the maximum voltage gain exceeds -29, it is safe to assume that proper adjustment of the potentiometer will result in oscillation. The output resistance of the inverting amplifier is very small. Therefore, we shall assume that it is negligible. Further inspection of Fig. 15-3 would seem to indicate that the amplifier's input resistance is also adequate.

\[ R_{in} = R_1 = 33 \, \text{k\Omega} \gg R = 3.3 \, \text{k\Omega} \]

Now we may draw on Eq. 15-10 to find the frequency of oscillation.

\[ f_o = \frac{1}{2\pi \sqrt{RC}} = \frac{1}{2\pi \sqrt{6 \times (3.3 \, \text{k\Omega})(0.1 \, \mu\text{F})}} = 197 \text{ Hz} \]

The phase-shift oscillator clearly demonstrates the basic principles behind the audio-frequency harmonic oscillator. However, it is not an extremely popular circuit. It is difficult to adjust or trim its frequency of oscillation. A far more popular circuit is the Wien bridge oscillator.

15-4 Wien Bridge Oscillators

The "heart" of all the harmonic oscillators consists of their frequency-determining feedback networks. The particular feedback circuit arrangement gives rise to the name of a particular oscillator. Examples include the Pierce, Hartley, Colpitts, Clapp, and Wien bridge oscillators. A Wien bridge oscillator that employs an op amp has been illustrated in Fig. 15-4(a). The others are discussed later.

The Wien bridge oscillator employs a lead–lag network. The phase shift across the network lags with increasing frequency and leads with decreasing frequency. As can be seen in Fig. 15-4, the lead–lag network consists of a parallel RC network in series with a series RC network. At a particular frequency, the phase shift across the network is 0°. Therefore, the feedback network is connected to the op amp's noninverting input terminal. The basic topology was shown in Fig. 15-1(b).

The frequency-determining feedback network has been redrawn in Fig. 15-4(b). To analyze it, we shall follow the same procedure applied to the RC phase-shift network. First, we shall find the parallel equivalent impedance of \( R_1 \) and \( C_1 \).

\[ Y = G + jB = \frac{1}{R_1} + j\omega C_1 = \frac{1 + j\omega R_1 C_1}{R_1} \]
and

\[ Z = \frac{1}{Y} = \frac{R_1}{1 + j\omega R_1 C_1} \]

By employing voltage division, we shall develop our equation for the network's voltage gain (\( \beta \)). Hence

\[ \beta = \frac{V_2}{V_1} = \frac{R_1/((1 + j\omega R_1 C_1,R_2 + 1/j\omega C_2 + R_1/((1 + j\omega R_1 C_1) = \frac{R_1}{(1 + j\omega R_1 C_1,\left[ R_2(j\omega C_2)(1 + j\omega R_1 C_1) + 1 + j\omega R_1 C_1 + j\omega R_1 C_2, j\omega C_2(1 + j\omega R_1 C_1) \right]}} \]

Continuing with algebraic manipulation, we eventually arrive at

\[ \beta = \frac{R_1}{j\omega C_2(1 + j\omega R_1 C_1, j\omega R_1 C_2, j\omega R_1 C_2 - \omega^2 R_1 R_2 C_1 C_2 + 1 + j\omega R_1 C_1 + j\omega R_1 C_2, j\omega R_1 C_2, j\omega R_1 C_2 - \omega R_1 C_2, j\omega R_1 C_2, \omega R_1 C_2 + \omega R_1 C_2 + R_1 C_2, j(\omega^2 R_1 R_2 C_1 C_2 - 1) \right) \]

\[ \approx \frac{R_1}{j(1 - \omega^2 R_1 R_2 C_1 C_2) + \omega R_1 C_1 + R_2 C_2 + R_1 C_2} - j \]

\[ \omega R_1 C_2 + j(\omega^2 R_1 R_2 C_1 C_2 - 1) \]

\[ \text{(15-11)} \]
At the frequency of oscillation ($f_o$ or $\omega_o$) the imaginary term (in the denominator) must be equal to zero, and the magnitude of $\beta$ must be a positive real number. This means that the phase shift across the network will be 0°. Hence

$$\omega_o^2 R_1 R_2 C_1 C_2 - 1 = 0$$

$$\omega_o^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

(15-12)

The frequency of oscillation in hertz is given by

$$f_o = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

(15-13)

where $f_o$ is the Wien bridge oscillator frequency of oscillation in hertz.

Generally, to determine the magnitude of $\beta$ at $f_o$, we must substitute Eq. 15-12 for $\omega_o$ into our equation for $\beta$ (Eq. 15-11). However, although this approach will work, we can avoid additional algebra by making some simple observations. Specifically, the imaginary term is zero at $f_o$, and since $\omega_o$ appears in the numerator and the denominator, we may cancel them. The development is as follows:

$$\beta = \frac{\omega_o R_1 C_2}{\omega_o (R_1 C_1 + R_2 C_2 + R_1 C_2) + j0}$$

$$= \frac{R_1 C_2}{R_1 C_1 + R_2 C_2 + R_1 C_2}$$

$$= \frac{R_1 C_2}{R_1 C_1} + \frac{R_2 C_2}{R_1 C_2} + \frac{R_1 C_2}{R_1 C_2}$$

$$\beta = \frac{1}{1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}}$$

(15-14)

Quite often the Wien bridge feedback network is designed such that the resistors and capacitors are equal in value. Hence

$$R_1 = R_2 = R \quad \text{and} \quad C_1 = C_2 = C$$

In this case, the equations for $f_o$ and $\beta$ (at $f_o$) simplify further.
\[ f_o = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}} \]
\[ = \frac{1}{2\pi \sqrt{R^2 C}} \]

\[ f_o = \frac{1}{2\pi RC} \bigg|_{R_1 = R_2 = R \text{ and } C_1 = C_2 = C} \]

(15-15)

Further,

\[ \beta = \frac{1}{1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}} = \frac{1}{1 + \frac{R}{R} + \frac{C}{C}} \]

\[ \beta = \frac{1}{3} \bigg|_{R_1 = R_2 = R \text{ and } C_1 = C_2 = C} \]

(15-16)

**EXAMPLE 15-2**

Analyze the Wien bridge oscillator given in Fig. 15-4(a). Specifically, determine its frequency of oscillation and determine if the noninverting amplifier has enough gain capability to ensure oscillation.

**SOLUTION** First, we note that the frequency-determining feedback elements are equal in value. Therefore, we may use Eq. 15-15 to determine the frequency of oscillation.

\[ f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi (1.5 \text{ k}\Omega)(0.1 \mu\text{F})} = 1.06 \text{ kHz} \]

From Eq. 15-16 we see that the feedback factor \( \beta \) is \( \frac{1}{3} \). Therefore, the noninverting amplifier must have a voltage gain which is slightly greater than 3 to initiate oscillation and a gain of 3 to sustain the oscillation. The gain can be varied by adjusting potentiometer \( R_3 \). When \( R_3 \) is fully counterclockwise,

\[ A_v = 1 + \frac{R_4 + R_5}{R_3} = 1 + \frac{2.7 \text{ k}\Omega + 0 \text{ k}\Omega}{1.5 \text{ k}\Omega} = 2.8 \]

which is slightly below the minimum required value. However, when potentiometer \( R_3 \) is fully clockwise,

\[ A_v = 1 + \frac{R_4 + R_5}{R_3} = 1 + \frac{2.7 \text{ k}\Omega + 1 \text{ k}\Omega}{1.5 \text{ k}\Omega} = 3.47 \]

which should be more than adequate.  

As we saw in Example 15-2 potentiometer \( R_3 \) can be adjusted to give our amplifier the required gain. However, if \( R_3 \) is adjusted a little low, the voltage gain will be slightly less than 3. Therefore, when power is first applied, the oscillations will die out or fail to start. If potentiometer \( R_3 \) is adjusted a little high, the voltage
gain will be slightly greater than 3. Under this condition, we can guarantee that the circuit oscillations will build up when power is applied. However, the oscillations will continue to grow until the output waveform is distorted. The oscillator’s output waveform will be clipped on the positive and negative peaks as the amplifier enters saturation.

The ideal situation would be an amplifier that has a voltage gain which is initially larger than 3 (a loop gain greater than unity) and reduces to 3 as the output level grows (a loop gain of unity). **Adaptive negative feedback** offers us a solution. One such scheme has been depicted in Fig. 15-5(a). Diodes $D_1$ and $D_2$ are signal diodes (such as the 1N914 or the 1N4148). Let us examine the circuit operation.

When power is first applied, electrical noise with a vast spectral content will be produced. The frequency-determining network will “pick out” $f_0$, and the circuit will begin to oscillate at that frequency. Since the output signal is at a low level (i.e., a few millivolts), diodes $D_1$ and $D_2$ will not conduct. Therefore, $R_3$ is in series with an open circuit and has no effect. The feedback network effectively consists of $R_4$ alone, and the voltage gain is

$$A_v = 1 + \frac{R_4}{R_3} = 1 + \frac{3.3 \text{ k}\Omega}{1.5 \text{ k}\Omega} = 3.2$$

A voltage gain of 3.2 should be more than adequate to allow the oscillations to build up. As the output level builds up, more voltage will be developed across $R_4$. When the peak voltage drops across $R_4$ reaches approximately 0.5 V, the diodes will begin to conduct. Diode $D_1$ conducts when the output is positive, and diode $D_2$ conducts when the output is negative. The diodes will begin to go into conduction when the output level reaches approximately 0.727 V.

Since the diodes are slightly conducting on the positive and negative peaks, the diodes (and $R_3$) will be in shunt with feedback resistor $R_4$. This will lower the amplifier’s voltage gain. As the output voltage continues to grow, the positive and negative peaks will drive the diodes further into conduction. Eventually, the diodes will conduct hard enough such that the voltage gain will be reduced to 3.

Predicting the required output voltage to cause adequate diode conduction is a rather difficult nonlinear circuit analysis problem. Specific numerical answers are a strong function of the individual diode characteristics. Therefore, such analysis holds questionable merit. The “real-world” solution is to make $R_3$ adjustable. The potentiometer is used to adjust the output voltage for minimal distortion.

Contrast this. The setting of potentiometer $R_5$ in Fig. 15-4(a) is critical to ensure oscillation. The circuit given in Fig. 15-5(a) is guaranteed to oscillate. Potentiometer $R_3$ is merely used to adjust the output for minimum distortion.

The lower the output level, the less the distortion will be. The potentiometer will affect both the output amplitude and the distortion present in the output. Quite often, if potentiometer $R_3$ in Fig. 15-5(a) is adjusted too low, the output will appear to exhibit crossover distortion. In this case the diodes are producing the distortion as they go in and out of conduction. One remedy is to increase the setting of potentiometer $R_5$. However, this is occasionally undesirable, as the output level will also be increased.

If we add another op amp and extract the output signal from across the parallel combination of $R_1$ and $C_1$, the output will contain less distortion. This occurs because of the filtering action produced by $R_1$ and $C_1$. This scheme is illustrated in Fig.
FIGURE 15-5  Adding adaptive negative feedback: (a) using a diode network to provide adaptive negative feedback; (b) providing a low-distortion output with adjustable amplitude.
Observe that the noninverting amplifier is one-half of a 747 dual (741) op amp. The use of a noninverting amplifier produces negligible loading on the feedback network. In this circuit, potentiometer \( R_s \) is adjusted to provide minimal output distortion. Potentiometer \( R_s \) is then used to adjust the output amplitude.

An alternative approach to the use of diodes to provide adaptive negative feedback requires the use of a JFET. The JFET can be used as a voltage variable resistor (VVR). Specifically, the JFET's drain-to-source ac resistance can be controlled by the dc bias impressed between its gate and source terminals. It offers the advantage of "softer" gain control and improved linearity. From an oscillator standpoint, this means less output distortion.

### 15-5 JFETs as Voltage Variable Resistors

Although our immediate concern is providing improved adaptive negative feedback for our Wien bridge oscillator, the use of the JFET as a voltage-variable resistor merits some additional discussion. The VVR is often employed in voltage-controlled attenuator circuits and in automatic gain control (AGC) applications.

In all of our previous work, we have operated our FETs in their pinch-off or constant-current region of operation [refer to Fig. 15-6(a)]. Recall that the locus of points is defined by

\[
|V_{DS}| + |V_{GS}| = |V_{GS(OFF)}| \quad (15-17)
\]

As long as the operating points lie to the right of this boundary line, the JFET is in its pinch-off region. Under this condition, the drain current is given by

\[
I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(OFF)}} \right] \quad (15-18)
\]

However, if we operate the JFET to the left of the boundary line given by Eq. 15-17, we are in its ohmic region of operation. In this case, the drain current is defined by a new relationship,

\[
I_D = \frac{2I_{DSS}}{V_{GS(OFF)}} \left( V_{GS} - V_{GS(OFF)} - \frac{V_{DS}}{2} \right) V_{DS} \quad (15-19)
\]

For very small values of \( V_{DS} \), we can expand the region about the origin as shown in Fig. 15-6(b). As we can see, the \( V-I \) characteristics are fairly linear, and their slopes are controlled by the magnitude of \( V_{GS} \). The greater the slope, the lower the resistance. This becomes clear when we compare the \( V-I \) characteristics of various resistors [Fig. 15-6(c)] with Fig. 15-6(b).

The smallest value of drain-to-source resistance occurs when \( V_{GS} \) is zero and is designated as \( r_{DS(ON)} \). It has been defined graphically in Fig. 15-7. Hence

\[
r_{DS(ON)} = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS} = 0} \quad (15-20)
\]

The data sheets of FETs which are intended to be used as VVRs or switches often include the parameter \( r_{DS(ON)} \). Its value is typically very small, ranging from a few hundred ohms to less than 1 \( \Omega \).

As \( V_{GS} \) becomes more negative, the value of \( r_{DS} \) becomes greater. Note that the
parameter $r_{DS}$ should not be confused with $r_0$. The parameter $r_{DS}$ refers to the (typically) small drain-to-source resistance in the ohmic region, while $r_0$ refers to the much larger drain-to-source resistance in the pinch-off region.

It should be clear that the reciprocal of the drain-to-source resistance ($r_{DS}$) yields the drain-to-source conductance ($g_{DS}$). Hence

$$g_{DS} = \frac{1}{r_{DS}} \quad (15-21)$$

and

$$g_{DS} = \frac{\partial I_D}{\partial V_{DS}} \quad (15-22)$$
where \( \frac{\partial I_D}{\partial V_{DS}} \) is the partial derivative (rate of change) of the drain current with respect to the drain-to-source voltage.

To obtain a functional relationship for \( g_{DS} \), we must take the partial derivative of Eq. 15-19. Mathematically uninitiated students may ignore the calculus and go directly to Eq. 15-24.

First, we distribute \( V_{DS} \).

\[
I_D = \frac{2I_{DSS}}{V_{GSOFF}^2} \left[ V_{GS} - V_{GSOFF} - \frac{V_{DS}}{2} \right] V_{DS}
\]

\[
= \frac{2I_{DSS}}{V_{GSOFF}^2} \left[ V_{GS}V_{DS} - V_{GSOFF}V_{DS} - \frac{V_{DS}^2}{2} \right]
\]

Taking the derivative yields

\[
g_{DS} = \frac{\partial I_D}{\partial V_{DS}} = \frac{2I_{DSS}}{V_{GSOFF}^2} \frac{\partial}{\partial V_{DS}} \left[ V_{GS}V_{DS} - V_{GSOFF}V_{DS} - \frac{V_{DS}^2}{2} \right]
\]

\[
= \frac{2I_{DSS}}{V_{GSOFF}^2} \left[ V_{GS} - V_{GSOFF} - V_{DS} \right]
\]

In Section 5-13, an equation (Eq. 5-11) was developed for the transconductance \( g_{mo} \) of a JFET when its \( V_{GS} \) is zero. Recalling that \( g_{f0} \) is the symbol used by many manufacturers, we have

\[
g_{f0} = -\frac{2I_{DSS}}{V_{GSOFF}^2}
\]

Substituting this relationship into our equation for \( g_{DS} \), we arrive at

\[
g_{DS} = \frac{2I_{DSS}}{V_{GSOFF}^2} \left[ V_{GS} - V_{GSOFF} - V_{DS} \right]
\]

\[
= -\frac{2I_{DSS}}{V_{GSOFF}} \left[ 1 - \frac{V_{GS}}{V_{GSOFF}} + \frac{V_{DS}}{V_{GSOFF}} \right]
\]

\[
= g_{f0} \left[ 1 - \frac{V_{GS}}{V_{GSOFF}} + \frac{V_{DS}}{V_{GSOFF}} \right]
\]

(15-23)
To ensure linearity in $g_{DS}$, the FET must remain in its ohmic region of operation, and $V_{DS}$ must be kept small. From Eq. 15-17,

$$|V_{DS}| \ll |V_{GS(OFF)}| - |V_{GS}|$$

Hence we obtain the approximation given in

$$g_{DS} = g_{f0} \left( 1 - \frac{V_{GS}}{V_{GS(OFF)}} \right) \quad \text{for } |V_{DS}| \ll |V_{GS(OFF)}| - |V_{GS}| \quad (15-24)$$

$$g_{DS} = \frac{1}{r_{ds(on)}} \left( 1 - \frac{V_{GS}}{V_{GS(OFF)}} \right) \quad \text{for } |V_{DS}| \ll |V_{GS(OFF)}| - |V_{GS}| \quad (15-25)$$

The constraint on $V_{DS}$ is very important. Disregarding it has resulted in VVR circuits that have produced intolerable amounts of distortion and has given the JFET VVR an often undeserved bad reputation.

**EXAMPLE 15-3**

A 2N5458 n-channel JFET is to be used as a VVR. Its $r_{ds(on)}$ is not given, but we do know that its minimum $V_{GS(OFF)}$ is $-2$ V, and its minimum $|V_{f0}|$ is 1500 $\mu$S. If $V_{DS}$ is kept very small, determine $r_{DS}$ if $V_{GS}$ is 0, -0.4, -0.8, -1.2, -1.6, and -1.999 V.

**SOLUTION** Since we do not know $r_{ds(on)}$, we shall employ Eq. 15-24. We recall that $|V_{f0}|$ is approximately equal to $g_{f0}$. Hence, for a $V_{GS}$ of 0 V,

$$g_{DS} = g_{f0} \left( 1 - \frac{V_{GS}}{V_{GS(OFF)}} \right)$$

$$= (1.5 \times 10^{-3} \text{ S}) \left( 1 - \frac{0 \text{ V}}{-2 \text{ V}} \right) = 1.5 \text{ mS}$$

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{1.5 \text{ mS}} = 667 \Omega$$

and for a $V_{GS}$ of -0.4 V,

$$g_{DS} = g_{f0} \left( 1 - \frac{V_{GS}}{V_{GS(OFF)}} \right)$$

$$= (1.5 \times 10^{-3} \text{ S}) \left( 1 - \frac{-0.4 \text{ V}}{-2 \text{ V}} \right) = 1.2 \text{ mS}$$

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{1.2 \text{ mS}} = 833 \Omega$$

The rest of the calculations are very similar and have been summarized in Table 15-1. A graph of the results has been given in Fig. 15-8.
TABLE 15-1
$r_{DS}$ Values for Example 15-3

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$r_{DS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>667 Ω</td>
</tr>
<tr>
<td>-0.4</td>
<td>833 Ω</td>
</tr>
<tr>
<td>-0.8</td>
<td>1.11 kΩ</td>
</tr>
<tr>
<td>-1.2</td>
<td>1.67 kΩ</td>
</tr>
<tr>
<td>-1.6</td>
<td>3.33 kΩ</td>
</tr>
<tr>
<td>-1.999</td>
<td>1.33 MΩ</td>
</tr>
</tbody>
</table>

FIGURE 15-8  Graph of the $r_{DS}$ values for Example 15-3.
Amplitude-Stabilized Wien Bridge Oscillator Using a VVR

The Wien bridge oscillator given in Fig. 15-9 employs a JFET as a VVR. The $r_{DS}$ of the JFET is used to control the voltage gain of the noninverting amplifier. Diodes $D_1$ and $D_2$ are used to form a half-wave rectifier. When the output voltage becomes sufficiently large, it is converted to negative pulsating dc. Capacitor $C_3$ is used as a filter to "smooth" the pulsating dc to provide a constant dc bias voltage across the JFET's gate-to-source terminals. Resistor $R_2$ is used to pull the gate of the JFET to ground. This ensures a $V_{GS}$ of zero when the diodes are not conducting.

When power is first applied, the oscillations will begin to build up. The peak amplitude of the output voltage will be insufficient to cause diodes $D_1$ and $D_2$ to go into conduction. Therefore, they will act like open circuits, and $V_{GS}$ will be zero. The JFET's drain-to-source resistance $r_{DS}$ will be its minimum value $r_{DS_{ON}}$. This will cause the voltage gain to be at its maximum value. This ensures a loop gain that is greater than unity.

The oscillations will continue to build up. When the (negative) peak output voltage reaches approximately 5.8 V (5.1 V + 0.7 V), the diodes ($D_1$ and $D_2$) will

FIGURE 15-9 Amplitude-stabilized Wien bridge oscillator using a VVR.
both go into conduction. Any further increases in the peak output voltage will develop a negative voltage $V_{GS}$ across the JFET. This will cause its $r_{DS}$ to increase.

The increase in $r_{DS}$ will increase the total resistance from the op amp's inverting input to ground. This will reduce the voltage gain. The output voltage will continue to grow, and the voltage gain will continue to decrease until the loop gain is reduced to unity. When this condition is reached, the output amplitude will be stabilized.

To further our insight, let us analyze Fig. 15-9 in greater detail. The frequency of oscillation can be determined from Eq. 15-13.

$$f_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

$$= \frac{1}{2\pi\sqrt{(1 \text{ k}\Omega)(15 \text{ k}\Omega)(0.15 \mu\text{F})(0.01 \mu\text{F})}}$$

$$= 1.06 \text{ kHz}$$

Observe that the frequency of oscillation is equal to that of the Wien bridge oscillator given in Fig. 15-5(a). The capacitor and resistor values used in Fig. 15-9 were purposely changed to yield the same $f_o$ and simultaneously lower the $\beta$ of the feedback network. From Eq. 15-14,

$$\beta = \frac{1}{1 + R_2/R_1 + C_1/C_2} = \frac{1}{1 + 15 \text{ k}\Omega/1 \text{ k}\Omega + 0.15 \mu\text{F}/0.01 \mu\text{F}}$$

$$= \frac{1}{31}$$

Obviously, the $\beta$ of Fig. 15-9 is much smaller than the $\beta$ of \frac{1}{3} that occurs when the feedback resistors ($R_1$ and $R_2$) and capacitors ($C_1$ and $C_2$) are equal in value [Fig. 15-5(a)]. The smaller $\beta$ requires a larger voltage gain (31 in this instance) to provide a loop gain of unity.

Raising the required voltage gain reduces the fraction of the output voltage that appears across $R_4$ and the drain-to-source of the JFET. This ensures that a small ac voltage will appear across the JFET, and promotes linearity.

If the feedback resistors $R_3$ and $R_4$ are selected properly, the voltage gain of 31 should be achieved with the JFET's $r_{DS}$ being close to its $r_{DS(on)}$ value. This means that $V_{GS}$ will be close to zero. In this case, the negative peak output voltage will be

$$v_{\text{out(peak, neg)}} = -(V_{D1} + V_{D2}) + V_{GS}$$

In Fig. 15-9 the negative peak output voltage will be approximately $-5.8$ V plus the value of $V_{GS}$ required for the circuit to stabilize. Allowing $-0.2$ V for $V_{GS}$, this would mean a negative peak output voltage of approximately $-6$ V. The positive peak will also be approximately 6 V.

The $R_3-C_3$ network will provide adequate filtering if its time constant is much, much larger than the period of the oscillation frequency. Thus

$$R_3 C_3 >> T$$

We have already determined that $f_o$ is 1.06 kHz. Hence

$$T = \frac{1}{f_o} = \frac{1}{1.06 \text{ kHz}} = 0.943 \text{ ms}$$

Therefore, in Fig. 15-9 we have
\[ R_5 C_3 = (100 \text{ k}\Omega)(1 \mu\text{F}) = 100 \text{ ms} >> 0.943 \text{ ms} \]

Obviously, \( R_5 \) and \( C_3 \) appear to be adequately sized.

The 2N5458 n-channel JFET has a transconductance \( g_{\text{f0}} \) which can range from 1500 to 5500 \( \mu\text{S} \). Hence

\[
r_{\text{DS(ON)-min}} = \frac{1}{g_{\text{f0}(\text{max})}} = \frac{1}{5500 \mu\text{S}} = 182 \Omega
\]

\[
r_{\text{DS(ON)-max}} = \frac{1}{g_{\text{f0}(\text{min})}} = \frac{1}{1500 \mu\text{S}} = 667 \Omega
\]

The range of possible \( r_{\text{DS(ON)}} \) values requires the use of potentiometer \( R_4 \) in the design. This allows us to trim in the circuit for optimal performance for any 2N5458 that might happen to be used. This is demonstrated in the following development.

Let us assume that we have a 2N5458 JFET with a \( g_{\text{f0}} \) of 1500 \( \mu\text{S} \) and the minimum \( V_{\text{GS(OFF)}} \) of \(-1\text{ V}\). In this case we shall allow the circuit to stabilize when \( V_{\text{GS}} \) reaches 10% of \( V_{\text{GS(OFF)}} \), or \(-0.1\text{ V}\). From Eq. 15-24,

\[
g_{\text{DS(min)}} = g_{\text{f0(min)}} \left[ 1 - \frac{V_{\text{GS}}}{V_{\text{GS(OFF)-min}}} \right]
\]

\[
= (1500 \mu\text{S}) \left( 1 - \frac{-0.1 \text{ V}}{-1 \text{ V}} \right) = 1.35 \text{ mS}
\]

\[
r_{\text{DS(max)}} = \frac{1}{g_{\text{DS(min)}}} = \frac{1}{1.35 \text{ mS}} = 741 \Omega
\]

A 2N5458 with the maximum \( g_{\text{f0}} \) of 5500 \( \mu\text{S} \) will also have the maximum \( V_{\text{GS(OFF)}} \) of \(-7\text{ V}\). In this case 10% of \( V_{\text{GS(OFF)}} \) is \(-0.7\text{ V}\). Thus

\[
g_{\text{DS(max)}} = g_{\text{f0(max)}} \left[ 1 - \frac{V_{\text{GS}}}{V_{\text{GS(OFF)-max)}} \right]
\]

\[
= (5500 \mu\text{S}) \left( 1 - \frac{-0.7 \text{ V}}{-7 \text{ V}} \right) = 4.95 \text{ mS}
\]

\[
r_{\text{DS(min)}} = \frac{1}{g_{\text{DS(max)}}} = \frac{1}{4.95 \text{ mS}} = 202 \Omega
\]

The peak output voltage in this case will be approximately 6.5 V. The reader should verify this.

**EXAMPLE 15-4**

Determine the "startup" voltage gain of the Wien bridge oscillator given in Fig. 15-9 if the 2N5458 has a \( g_{\text{f0}} \) of 1500 \( \mu\text{S} \) and a \( V_{\text{GS(OFF)}} \) of \(-1\text{ V}\). Also determine the "stabilized" voltage gain if \( V_{\text{GS}} \) is allowed to reach \(-0.1\text{ V}\) via the setting of potentiometer \( R_4 \) [see Fig. 15-10(a)].

**SOLUTION** From our previous work and Fig. 15-10(a), we see that \( r_{\text{DS(ON)}} \) is 667 \( \Omega \). Notice that the upper portion of the potentiometer has been denoted as \( R_{4A} \) and the lower portion as \( R_{4B} \). In this case the equivalent resistance from the inverting input to ground is

\[
R_T = R_{4A} + R_{4B} \parallel r_{\text{DS(ON)}}
\]

\[
= 209 \Omega + 1791 \Omega \parallel 667 \Omega = 695 \Omega
\]
FIGURE 15-10  Operation of the VVR in the Wien bridge oscillator:
(a) oscillator during startup; (b) stabilized oscillator.
and the corresponding (startup) voltage gain is

\[ A_v = 1 + \frac{R_3}{R_T} = 1 + \frac{22 \text{ k}\Omega}{695 \text{ } \Omega} = 32.7 \]

which is larger than the required 31 to sustain oscillation. When the peak output voltage reaches 5.9 V, \( V_{GS} \) will be equal to -0.1 V. The drain-to-source resistance \( r_{DS} \) will be 741 \( \Omega \). At this point \( R_T \) will be

\[ R_T = R_{4A} + R_{4B} \parallel r_{DSON} \]
\[ = 209 \Omega + 1791 \Omega \parallel 741 \Omega = 733 \Omega \]

and

\[ A_v = 1 + \frac{R_3}{R_T} = 1 + \frac{22 \text{ k}\Omega}{733 \Omega} = 31 \]

A (stabilized) voltage gain of 31 will provide a loop gain of unity, and the oscillations will be sustained [see Fig. 15-10(b)].

15-7 Adjusting the Frequency of the Wien Bridge Oscillator

Quite often it is desirable to have a harmonic oscillator that has an adjustable frequency of oscillation. In the case of the Wien bridge oscillator, this can be accomplished by adjusting one of the elements in the frequency-determining feedback network (e.g., \( R_1, R_2, C_1, \) or \( C_2 \)). However, varying any one of these components will change the \( \beta \) of the feedback network. If the \( \beta \) is changed, the loop gain will also change, and the oscillator will either start to distort or will cease to oscillate.

One alternative is to use a ganged potentiometer [see Fig. 15-11(a)]. The phantom lines are used to indicate that the rotors of the two potentiometers are mechanically tied together. The two potentiometers are electrically separate but are housed in a single package. This scheme will allow the frequency to be adjusted without changing the \( \beta \) of the feedback network. Therefore, distortion or a cessation of oscillations will be avoided. However, ganged potentiometers are relatively expensive and can be difficult to procure. A rather clever alternative is to utilize active negative feedback [see Fig. 15-11(b)].

The "main" amplifier is \( AR_1 \), and amplifier \( AR_2 \) provides voltage-gain compensation. The components utilized to achieve an adjustable output frequency are relatively inexpensive and easy to obtain. This makes the circuit given in Fig. 15-11(b) extremely attractive.

Observe that some constraints have been placed on the components. Specifically, resistors \( R_2, R_3, R_4, \) and \( R_5 \) are all equal in value. Capacitors \( C_1 \) and \( C_2 \) are also equal in value. These constraints make the operation of the circuit easier to understand. From a hardware standpoint, these constraints also minimize the number of different components required to build the circuit. This is often an advantage.

From Eq. 15-13,

\[ f_0 = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}} \left| \frac{C_1 \cdot C_2 \cdot C \cdot R}{C_1 + C_2 + C \cdot R} \right| = \frac{1}{2\pi \sqrt{R_1 R}} \]
FIGURE 15-11 Adjusting the frequency of the Wien bridge oscillator: (a) using ganged potentiometers; (b) using active negative feedback and a single potentiometer.

and from Eq. 15-14,

$$\beta = \frac{1}{1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}} = \frac{1}{2 + \frac{R}{R_1}} \bigg|_{C_1 = C_2 = C, R_2 = R}$$

As $R_1$ is increased, $f_0$ is lowered and $\beta$ is increased. Conversely, as $R_1$ is decreased, $f_0$ is increased and $\beta$ is decreased.

Since the $\beta$ of the frequency-determining feedback network changes as $R_1$ is varied to change the frequency, amplifier AR2 has been added to adjust simultaneously the voltage gain of AR1. The intent is to keep the loop gain at unity. To see how this works, we must find the equation for the voltage gain of the amplifier system.
The basic amplifier circuit has been given in Fig. 15-12(a). To simplify our analysis, we draw on the substitution and superposition theorems.

The substitution theorem allows us to split \( v_{in} \) into equivalent signal sources [see \( v_{in1} \) and \( v_{in2} \) in Fig. 15-12(b)]. Now we can apply the superposition theorem.

In Fig. 15-12(c) we have set \( v_{in2} \) equal to zero. Since the input to \( AR_2 \) is zero, its output will also be zero. If we recall that zero volts is ground, we may use the substitution theorem to arrive at the equivalent circuit indicated in Fig. 15-12(c). Obviously, \( AR_1 \) will act as a noninverting amplifier, and

\[
v'_{out} = \left( 1 + \frac{R}{R} \right) v_{in1} = 2v_{in1}
\]

In Fig. 15-12(d) we have set \( v_{in1} \) to zero. By inspection we can see that \( AR_1 \) and \( AR_2 \) serve as two cascaded inverting amplifiers. Recalling that the overall voltage gain of a cascaded amplifier system is given by the product of the individual stage gains, we obtain the following result:

\[
v''_{out} = \left( -\frac{R}{R_1} \right) \left( -\frac{R}{R} \right) v_{in2} = \frac{R}{R_1} v_{in2}
\]

Adding our results produces our equation for \( v_{out} \):

\[
v_{out} = v'_{out} + v''_{out} = 2v_{in1} + \frac{R}{R_1} v_{in2}
\]

and since

\[
v_{in1} = v_{in2} = v_{in}
\]

the voltage gain may be found by dividing both sides by \( v_{in} \). Hence

\[
v_{out} = 2v_{in} + \frac{R}{R_1} v_{in} = \left( 2 + \frac{R}{R_1} \right) v_{in}
\]

\[
A_v = \frac{v_{out}}{v_{in}} = 2 + \frac{R}{R_1}
\]

Now we can see that the loop gain is

\[
\beta A_v = \frac{1}{2 + R/R_1} \left( 2 + \frac{R}{R_1} \right) = 1
\]

Consider this result. If we desire to increase \( f_o \), we must reduce \( R_1 \). This will lower the \( \beta \) of the frequency-determining feedback network. However, this will increase the voltage gain of the inverting amplifier \( AR_2 \), which serves to raise the voltage gain of the overall amplifier system. The increase in the amplifier gain will counteract the decrease in \( \beta \). Therefore, the loop gain will remain at unity, and the oscillations will be sustained.

A complete Wien bridge oscillator circuit that is based on this design approach has been given in Fig. 15-13. Although three op amps are used, they are all contained within the same 14-pin package - an LM324 quad op amp. Amplifier \( AR_1 \) serves as the main amplifier. Amplifier \( AR_2 \) provides the gain compensation. Amplifier \( AR_3 \) is used to provide additional voltage gain on the output signal. This allows us to have a relatively wide range of output signal amplitude adjustment.

In operation, potentiometer \( R_3 \) is used to adjust the output signal for minimum distortion. Potentiometer \( R_2 \) is used to determine the frequency of oscillation. Po-
FIGURE 15-12 Analyzing the adaptive negative feedback.
The distortion potentiometer $R_{11}$ may then be used to adjust the output signal amplitude. In practice, the distortion potentiometer ($R_7$) will be adjusted when the oscillator circuit is initially placed into service. It should not have to be adjusted again.

**EXAMPLE 15-5**

Determine the minimum and maximum frequency of oscillation of the Wien bridge oscillator given in Fig. 15-13. In the laboratory it was determined that when $R_7$ was adjusted for minimal output distortion, a 12-V peak sine wave was produced at $AR_3$'s output. Determine the range of output amplitudes available at $AR_3$'s output.
SOLUTION Using the subscripts employed in Fig. 15-13, we obtain our equation

\[
\omega_0 = \frac{1}{2\pi \sqrt{R_1 R_3}} = \frac{1}{2\pi (0.05 \, \mu F) \sqrt{(4.7 \, k\Omega)(10 \, k\Omega)}}
\]

= 464 Hz

This frequency will be obtained when \( R_2 \) is adjusted fully clockwise. When \( R_1 \) is fully counterclockwise, its full 20 k\( \Omega \) of resistance will be in the circuit. Hence

\[
\omega_0 = \frac{1}{2\pi \sqrt{(R_1 + R_2)R_3}}
\]

\[
= \frac{1}{2\pi (0.05 \, \mu F) \sqrt{(4.7 \, k\Omega + 20 \, k\Omega)(10 \, k\Omega)}}
\]

= 203 Hz

Potentiometer \( R_{11} \) and resistor \( R_{10} \) form a voltage divider. All potentiometers will exhibit a small amount of "end resistance" when they are adjusted to the ends of their travel. The use of \( R_{10} \) helps to minimize this effect and allows us to adjust the output voltage to nearly zero. When \( R_{11} \) is fully clockwise, we have the situation shown in Fig. 15-13(b). If we apply Thévenin's theorem, we find that

\[
R_{TH} = R_{10} \parallel R_{11} = 470 \, \Omega \parallel 5 \, k\Omega = 430 \, \Omega
\]

\[
v_{th} = \frac{R_{11}}{R_{10} + R_{11}} \cdot v_{out(AR1)} = \frac{5 \, k\Omega}{470 \, \Omega + 5 \, k\Omega} (12 \, V) = 11 \, V
\]

and since \( R_{TH} \) forms part of the equivalent resistance in series with \( AR_3 \)'s inverting input, we have

\[
v_{out(peak)} = -\frac{R_{14}}{R_{TH} + R_{12}} \cdot v_{th} = -\frac{68 \, k\Omega}{430 \, \Omega + 51 \, k\Omega} (11 \, V)
\]

\[
= -14.5 \, V \rightarrow a \, magnitude \, of \, 14.5 \, peak
\]

The maximum peak output voltage is approximately 14.5 V. However, it is quite likely that the op amp's output will saturate before this peak is reached. A conservative estimate would rate our circuit as capable of delivering a peak output voltage of at least 13 V. ■

15-8 High-Frequency Harmonic Oscillators

Quite often, harmonic oscillators are required to oscillate at frequencies considerably above the audio-frequency range. The possibilities encompass 20 kHz to several gigahertz. We restrict our discussion to oscillators which operate in the range 100 kHz to 30 MHz. Higher-frequency oscillators are best left to studies of communications electronics circuitry.

The use of \( RC \) harmonic oscillator circuits becomes impractical at high frequencies. With a little reflection, we recall that the frequency of oscillation is inversely proportional to the size of the capacitors employed in the frequency-determining
feedback network. Consequently, at high frequencies the size of the capacitors must shrink dramatically. When capacitors of only a few picofarads are used, stray capacitances (which are also on the order of a few picofarads) can detune the oscillator or even prohibit oscillation. Therefore, it becomes necessary to use alternative frequency-determining feedback networks. The most common approach is to use series and/or parallel resonant networks.

Resonant circuits require the use of capacitors and inductors (coils). Inductors tend to be impractical at low (e.g., audio) frequencies, but work quite well in RF applications. Further, resonant circuits tend to offer much sharper filtering than do the RC networks considered previously. This can make our work easier. Specifically, adaptive negative feedback circuitry may not be required. (Typically, some form will be used, but its design is not as critical.) This is true because the narrow frequency response of the resonant circuits tends to filter out the harmonics that may be produced by nonlinearities within the amplifier. However, there are other considerations.

Generally, discrete rather than integrated circuits are preferred. High-frequency, high-performance linear integrated circuits are available, but they tend to be relatively expensive. Consequently, discrete BJT and JFET amplifiers are often the most cost-effective approach.

As a result, we have several design details to attend to. For example, to ensure good frequency stability we must provide good bias stability. This can mean that we must include temperature-compensation schemes in our bias circuits. Power supply decoupling also becomes more demanding in RF applications. If we are not careful, the RF produced by the oscillator can "talk" to all the other circuits within the system via the power supply connections.

To understand high-frequency oscillators, we must first understand series and parallel resonant circuits. A brief review of their characteristics is provided in the next section. Some students may wish to review their circuit analysis textbook at this point.

15-9 Series and Parallel Resonant Circuits

A series resonant circuit has been illustrated in Fig. 15-14(a). All series resonant circuits contain capacitance, inductance, and resistance. The resistance is often inherent within the coil and need not be a separate component. From basic circuit theory we recall that inductive reactance is directly proportional to the frequency of excitation.

\[ jX_L = j2\pi fL \]

Capacitive reactance is inversely proportional to the frequency of the excitation.

\[ -jX_C = \frac{1}{j2\pi fC} \]

At one particular frequency (the resonant frequency \( f_0 \)) the magnitude of the inductive reactance and the magnitude of the capacitive reactance will be equal. Using this definition, we may solve for the resonant frequency in terms of the inductance and capacitance. At \( f_0 \), \( X_L = X_C = X \) and
\[ 2\pi f_o L = \frac{1}{2\pi f_o C} \]
\[ f_o^2 = \frac{1}{(2\pi)^2 LC} \]
\[ f_o = \frac{1}{2\pi \sqrt{LC}} \]

(15-26)

At resonance the impedance \(Z_o\) of the series resonant circuit is at its minimum since \(X_C\) and \(X_L\) cancel one another.

\[ Z_o = R + jX_L - jX_C = R + jX - jX = R \]

The net impedance is purely resistive and equal to \(R\). The graph of the impedance of a series resonant circuit versus frequency has been indicated in Fig. 15-14(b).

At frequencies below \(f_o\) the impedance is primarily capacitive. At frequencies

**FIGURE 15-14 Series resonant circuit.**
above \( f_0 \) the impedance is primarily inductive. At \( f_0 \) the impedance is at its minimum and resistive. (The phase angle is 0°.)

Below and above \( f_0 \) at the frequencies \( f_1 \) and \( f_2 \), respectively, the magnitude of the impedance increases to a value equal to the square root of 2 times \( R \). These two frequencies are used to define the bandwidth (BW) of the series resonant circuit.

\[
BW = f_2 - f_1
\]

(15-27)

Since the current through the series resonant circuit is inversely proportional to its impedance, we may also represent the frequency response as indicated in Fig. 15-14(c). When the current is reduced by a factor of approximately 0.707 at \( f_1 \) and \( f_2 \), it is reduced by 3 dB. Therefore, \( f_1 \) and \( f_2 \) are also referred to as the "3-dB down points." Consequently, Eq. 15-27 is really no different than our previous definition of bandwidth in Chapter 10.

The frequency selectivity of the series resonant circuit is inversely related to the quality factor \((Q)\) of the coil.

\[
BW = \frac{f_0}{Q}
\]

(15-28)

where \( BW \) = bandwidth (hertz)
\( f_0 \) = resonant frequency (hertz)
\( Q \) = coil's quality factor (dimensionless)

The \( Q \) of the coil has been defined by

\[
Q = \frac{X_L}{R}
\]

(15-29)

where \( Q \) is the coil's quality factor and should be determined at the frequency of interest. Generally, a very narrow bandwidth is highly desirable. This implies that we also desire coils with a very high (10 or more) \( Q \). The resistance \( R \) in Eq. 15-29 is associated with the coil. To emphasize this fact, the resistance shown in Fig. 15-14(a) has been enclosed in a dashed-line box with \( L \). The resistance \( R \) represents the dc and ac losses associated with all real inductors.

**Example 15-6**

The coil given in Fig. 15-14(a) has an inductance of 10 \( \mu \)H and a resistance of 6 \( \Omega \) in the frequency range of interest. The capacitor is a 0.0025-\( \mu \)F unit. Determine the resonant frequency \( f_0 \), the \( Q \) of the coil at \( f_0 \), the bandwidth of the circuit, and its impedance at resonance.

**Solution** From Eq. 15-26,

\[
f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(10 \ \mu \text{H})(0.0025 \ \mu \text{F})}} = 1.007 \text{ MHz}
\]
To find the $Q$ of the coil, we must first find the magnitude of $X_L$ at $f_o$.

$$X_L = 2\pi f_o L = 2\pi(1.007 \text{ MHz})(10 \mu\text{H}) = 63.3 \Omega$$

Now, from Eq. 15-29,

$$Q = \frac{X_L}{R} = \frac{63.3 \Omega}{6 \Omega} = 10.5$$

This would be classified as a high-$Q$ coil since its $Q$ is greater than 10. The bandwidth may be found from Eq. 15-28.

$$\text{BW} = \frac{f_o}{Q} = \frac{1.007 \text{ MHz}}{10.5} = 95.9 \text{ kHz}$$

The impedance of the series resonant circuit at $f_o$ is equal to the resistance of the coil. Hence

$Z_o = R = 6 \Omega$

A parallel resonant circuit has been given in Fig. 15-15(a). Once again, the effective series resistance of the coil has been indicated. In this case, the series resistance has been denoted as $R_p$.

If a high-$Q$ coil is used in a parallel resonant circuit, its resonant frequency ($f_o$) occurs when the magnitude of the capacitive reactance equals the magnitude of the inductive reactance. The resonant frequency is given by Eq. 15-26. A high-$Q$ coil is not an extremely restrictive constraint. Virtually all of the coils employed in our oscillator circuits will be of the high-$Q$ variety. (Again, the $Q$ should be specified at $f_o$.)

The impedance versus frequency has been depicted in Fig. 15-15(b). For frequencies below $f_o$, the inductive susceptance dominates and the circuit has an inductive

\[FIGURE 15-15 \text{ Parallel resonance: (a) parallel resonant circuit; (b) frequency response.} \]
characteristic. For frequencies above \( f_o \), the capacitive susceptance dominates and the circuit has a capacitive "flavor." The maximum impedance of a parallel resonant circuit occurs at \( f_o \) and is resistive. The impedance at resonance (with a high-\( Q \) coil) is given by

\[
R_p = Q^2 R_s
\]

(15-30)

where \( R_p \) = equivalent resistance of a parallel resonant circuit at \( f_o \)
\( Q \) = coil's quality factor (10 or more)
\( R_s \) = coil's internal (dc and ac) resistance

**EXAMPLE 15-7**

A 10-\( \mu \)H inductor has a \( Q \) of 200. (Its \( R_s \) is 0.316 \( \Omega \).) It is connected in parallel with a 0.0025-\( \mu \)F capacitor [see Fig. 15-15(a)] to form a resonant circuit. Determine its \( f_o \), its bandwidth, and its (resistive) impedance \( (R_p) \) at resonance.

**SOLUTION** Equation 15-26 may be used to determine \( f_o \).

\[
f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(10 \text{ } \mu\text{H})(0.0025 \text{ } \mu\text{F})}} = 1.007 \text{ MHz}
\]

Its bandwidth is given by Eq. 15-28.

\[
\text{BW} = \frac{f_o}{Q} = \frac{1.007 \text{ MHz}}{200} = 5.03 \text{ kHz}
\]

The impedance \( (Z) \) at resonance is \( R_p \) and is given by Eq. 15-30.

\[
R_p = Q^2 R_s = (200)^2 (0.316 \text{ } \Omega) = 12.6 \text{ k}\Omega
\]

From Example 15-7 we can see that at resonance a high-\( Q \) coil offers a high resistance and a very narrow bandwidth. Both of these characteristics are highly desirable in harmonic oscillator circuits. Consequently, the harmonic oscillators we consider in the next few sections will all incorporate high-\( Q \) coils.

**15-10 General LC Oscillator**

A number of the high-frequency harmonic oscillators can be represented by the general equivalent circuit given in Fig. 15-16(a). These oscillators are all characterized by the fact that they incorporate resonant circuits in their frequency-determining feedback networks. The three impedances \( Z_1, Z_2, \) and \( Z_3 \) are comprised of reactive circuit elements. The particular arrangement dictates the name of the oscillator. For example, when the impedances \( Z_1 \) and \( Z_3 \) are capacitors, and \( Z_3 \) is an inductor, we have a Colpitts oscillator. In this case an inverting amplifier is required (see Table 15-2). However, if the feedback elements are arranged such that \( Z_1 \) is an inductor while impedances \( Z_2 \) and \( Z_3 \) are capacitors, a noninverting amplifier may be employed. In some cases a crystal (XTAL) may be incorporated (see the Pierce oscillator in Table 15-2). The crystal is covered in Section 15-14.
FIGURE 15-16 General LC oscillator: (a) equivalent circuit; (b) determining \( \beta \); (c) determining \( A_w \).

Each of the oscillators listed in Table 15-2 is investigated in the sections to come. As we progress, the entries in the table will become clear. The table is by no means exhaustive. There are several variations and even fundamental oscillator types which are not mentioned. However, our objective is to provide insight into the basic considerations underlying the various LC oscillator types. By using the general LC model presented in Fig. 15-16(a), we can develop some fundamental relationships that can readily be extended to a number of specific LC oscillators.

<table>
<thead>
<tr>
<th>Oscillator Type</th>
<th>( Z_1 )</th>
<th>( Z_2 )</th>
<th>( Z_3 )</th>
<th>Amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hartley</td>
<td>( L )</td>
<td>( L )</td>
<td>( C )</td>
<td>Inverting</td>
</tr>
<tr>
<td></td>
<td>( L )</td>
<td>( C )</td>
<td>( L )</td>
<td>Follower</td>
</tr>
<tr>
<td>Colpitts</td>
<td>( C )</td>
<td>( C )</td>
<td>( L )</td>
<td>Inverting</td>
</tr>
<tr>
<td></td>
<td>( L )</td>
<td>( C )</td>
<td>( C )</td>
<td>Noninverting</td>
</tr>
<tr>
<td>Clapp</td>
<td>( C )</td>
<td>( C )</td>
<td>( LC ) series</td>
<td>Inverting</td>
</tr>
<tr>
<td>Pierce crystal</td>
<td>( C )</td>
<td>( C )</td>
<td>XTAL ( (L) )</td>
<td>Inverting</td>
</tr>
</tbody>
</table>
In Fig. 15-16(b) the feedback network has been redrawn. Our first step shall be to develop an equation for the feedback factor \( \beta \). By inspection of Fig. 15-16(b), we can see that we have simple voltage division between \( Z_2 \) and \( Z_3 \). Hence
\[
V_f = \frac{Z_2}{Z_2 + Z_3} V_{out}
\]
\[
\beta = \frac{V_f}{V_{out}} = \frac{Z_2}{Z_2 + Z_3} \tag{15-31}
\]

In Fig. 15-16(c) the feedback network has been redrawn once again. Our intent now is to determine its loading effect on the output of the amplifier. Observe that we have assumed that the input impedance of the amplifier is infinite. Specifically,
\[
Z_{in} \gg Z_2
\]
This is not merely an assumption but an important design objective in "real" oscillator circuits. Our next step will be to determine the equivalent load impedance \( Z_L \) across the amplifier's output. First we find the admittance.
\[
Y_L = \frac{1}{Z_1} + \frac{1}{Z_2 + Z_3} = \frac{Z_1 + Z_2 + Z_3}{Z_1(Z_2 + Z_3)}
\]
\[
Z_L = \frac{1}{Y_L} = \frac{Z_1(Z_2 + Z_3)}{Z_1 + Z_2 + Z_3}
\]

We now work to develop our equation for the amplifier's loaded voltage gain. We substitute in the result above at the appropriate point.
\[
V_{out} = \frac{Z_L}{Z_L + Z_{out}} A_{v(oc)} V_{in} = \frac{Z_1(Z_2 + Z_3)}{(Z_1 + Z_2 + Z_3)} A_{v(oc)} V_{in}
\]
\[
= \frac{Z_1(Z_2 + Z_3)}{(Z_1 + Z_2 + Z_3)} \left[ \frac{Z_1(Z_2 + Z_3)}{(Z_1 + Z_2 + Z_3)} + Z_{out} \right] A_{v(oc)} V_{in}
\]

Dividing both sides by \( V_{in} \) provides us with our equation for the loaded voltage gain.
\[
A_v = \frac{V_{out}}{V_{in}} = \frac{Z_1(Z_2 + Z_3)A_{v(oc)}}{Z_1(Z_2 + Z_3) + Z_{out}(Z_1 + Z_2 + Z_3)} \tag{15-32}
\]

The loop gain \( (\beta A_v) \) can be found by multiplying Eqs. 15-31 and 15-32. This leads us to
\[
\beta A_v = \left( \frac{Z_2}{Z_2 + Z_3} \right) \left( \frac{Z_1(Z_2 + Z_3)A_{v(oc)}}{Z_1(Z_2 + Z_3) + Z_{out}(Z_1 + Z_2 + Z_3)} \right)
\]
\[
= \frac{Z_1Z_2A_{v(oc)}}{Z_1(Z_2 + Z_3) + Z_{out}(Z_1 + Z_2 + Z_3)} \tag{15-33}
\]

At resonance,
\[
Z_1 + Z_2 + Z_3 = 0
\]
Therefore, we may use this fact to simplify our equation for the loop gain. Hence

$$\beta A_v = \frac{Z_1 Z_2 A_{v(oc)}}{Z_1 (Z_2 + Z_3)} = \frac{Z_2}{Z_2 + Z_3} A_{v(oc)}$$

Since

$$Z_1 + Z_2 + Z_3 = 0$$

then

$$Z_2 + Z_3 = -Z_1$$

and we may use this result to further simplify our equation for the loop gain. By substitution, we arrive at

$$\beta A_v = \frac{Z_2}{Z_2 + Z_3} A_{v(oc)} = \frac{Z_2}{-Z_1} A_{v(oc)} = \frac{Z_2}{Z_1} A_{v(oc)}$$

(15-34)

We can make some very powerful generalizations at this point. First, the frequency of oscillation can be determined by the following:

At $$f_o$$, $$Z_1 + Z_2 + Z_3 = 0$$

--- solve for $$f_o$$.

(15-35)

The amplifier gain must be large enough to ensure a loop gain larger than unity. Equation 15-36 states the requirement.

$$\beta A_v \geq 1$$

$$\frac{-Z_2}{Z_1} A_{v(oc)} \geq 1 \Rightarrow -A_{v(oc)} > \frac{Z_1}{Z_2}$$

$$A_{v(oc)} < -\frac{Z_1}{Z_2}$$

(15-36)

where $$A_{v(oc)}$$ is the required voltage gain to sustain oscillations.

Equations 15-35 and 15-36 will allow us to analyze LC oscillators such as the Colpitts, Clapp, Hartley, and Pierce oscillators without "reinventing the wheel" each time. This is illustrated in the sections that follow.

15-11 Colpitts Oscillators and Gate Leak Bias

A Colpitts oscillator circuit has been given in Fig. 15-17. The feedback network arrangement and the amplifier have been emphasized in Fig. 15-17(a). As we can see, $$Z_1$$ and $$Z_2$$ are capacitive reactances and $$Z_3$$ is an inductive reactance. In this case, an inverting amplifier is required. Observe that a common-source JFET amplifier has been indicated.

Capacitor $$C_3$$ is an input coupling capacitor. It serves to block the dc bias present at the drain of the JFET. Recall that a coil (e.g., $$L_1$$) is essentially a short circuit to dc. Therefore, capacitor $$C_3$$ is required to keep the large positive drain potential off the gate of the JFET. Resistor $$R_G$$ is used to reference the gate to ground. As we
shall see, resistor $R_G$ and $C_3$ also form a unique bias scheme referred to as gate leak bias. (The gate leak bias provides a form of adaptive negative feedback.)

Inductor $L_2$ is called a radio-frequency choke (RFC). Its dc resistance is low. Therefore, the drain will have a dc potential of approximately $V_{DD}$ volts. However, the inductive reactance of the RFC is very large at the frequency of oscillation. Its primary function is to keep the RF signal out of the power supply. Before we go any
further, let us begin our analysis of the Colpitts oscillator. A more conventional schematic diagram has been indicated in Fig. 15-17(b).

From Eq. 15-35, we recall that at the resonant frequency the reactances cancel one another. Hence

\[ Z_1 + Z_2 + Z_3 = 0 \]

We may use this relationship to determine the frequency of oscillation \( (f_o) \). By substitution,

\[ Z_1 + Z_2 + Z_3 = -j \left( \frac{1}{\omega C_1} + \frac{1}{\omega C_2} \right) + j\omega L_1 = 0 \]

\[ j\omega L_1 = j \left( \frac{1}{\omega C_1} + \frac{1}{\omega C_2} \right) = j \frac{C_1 + C_2}{\omega C_1 C_2} \]

\[ \omega^2 = \frac{1}{L_1 \left( \frac{C_1 C_2}{C_1 + C_2} \right)} \]

\[ f_o = \frac{1}{2\pi \sqrt{L_1 C_T}} \]  \hspace{1cm} (15-37)

where \( f_o = \) Colpitts oscillator frequency of oscillation (hertz)

\( L_1 = \) feedback inductance

\( C_T = \) series equivalent capacitance

\( = \frac{C_1 C_2}{C_1 + C_2} \)

Now that we have our equation for \( f_o \), we shall use Eq. 15-36 to determine the required amplifier gain to ensure sustained oscillations. Thus

\[ A_{v(\infty)} < \frac{-Z_1}{Z_2} = \frac{-1/j\omega C_1}{1/j\omega C_2} = \frac{-1}{j\omega C_1} \frac{1}{1} \]

\[ A_{v(\infty)} < -\frac{C_2}{C_1} \]  \hspace{1cm} (15-38)

where \( A_{v(\infty)} \) is the open-circuit voltage gain of the amplifier used in the Colpitts oscillator. This result indicates that the amplifier must be an inverting configuration, and the magnitude of its open-circuit voltage gain must be larger than the ratio of \( C_2 \) to \( C_1 \).

The open-circuit voltage gain may be determined from Fig. 15-18. Observe that the decoupling capacitor \( [C_s \text{ in Fig. } 15-17(b)] \) is a short circuit to the signal. This effectively places the RFC \( [L_2 \text{ in Fig. } 15-18(a)] \) in parallel with the JFET's output. Consequently, it forms part of the ac load across the JFET.

To find the open-circuit voltage gain, we must disconnect the load [refer to Fig. 15-18(b)]. Next, we note

\[ v_{out} = -g_m v_{gs} f_o \]

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FIGURE 15-18 Ac gain analysis: (a) basic ac equivalent circuit; (b) determining the open-loop voltage gain.

If we divide both sides by \( V_{gs} \), we obtain the open-circuit voltage gain.

\[
A_{(oc)} = -g_{m}R_{o}
\]

The use of Eqs. 15-37 and 15-38 and the relationship above is demonstrated in Example 15-8. However, before we proceed with the example, let us investigate the effects of the input coupling capacitor \( C_{3} \) and \( R_{G} \).

Radio-frequency oscillators are no different than audio-frequency oscillators in that some form of adaptive negative feedback is desirable. The sharp filtering action offered by the LC tuning networks greatly reduces the demands on the adaptive negative feedback scheme. Specifically, distortion is much less of a problem.

When the oscillator in Fig. 15-17 is first powered up, \( V_{GS} \) is 0 V. (This should not be too surprising since resistor \( R_{G} \) is used to pull the gate to ground.) Recall that when \( V_{GS} \) is zero the JFET has its maximum transconductance. Since its voltage gain is directly proportional to its transconductance, it will be at its maximum. Therefore, the loop gain will be large and the oscillations will begin to build up.

As the oscillations build up, so will the magnitude of the feedback voltage [see Fig. 15-19(a)]. When the positive peak of the feedback signal causes \( v_{GS} \) to reach approximately 0.5 V, the \( p-n \) junction between the gate and the source terminals will begin to conduct. A diode analogy will help [see Fig. 15-19(b)].

If we assume that the generator’s signal \( (v_{g}) \) reaches a peak value of 3 V, we see that the voltage across the capacitor reaches 2.4 V. This will occur very quickly because the forward resistance of the diode is small. As soon as \( v_{g} \) falls below 2.4 V, the diode will be reverse biased. Consequently, it will be nonconducting, or OFF. The discharge time constant will be much larger than the charge time constant, and the capacitor’s voltage will effectively remain at 2.4 V. When the peak value of \( v_{g} \) reaches \( -3 \) V, the peak reverse bias across the diode will reach \( -5.4 \) V [see Fig. 15-19(c)]. The average value of the reverse bias will be equal to the voltage across the capacitor \( -2.4 \) V, as indicated in Fig. 15-19(d).
**FIGURE 15-19** Gate leak bias: (a) the initially large loop gain allows the oscillations to build up; (b) the capacitor quickly charges to 2.4 V when the diode conducts; (c) the capacitor's discharge is very slow, causing the negative peak reverse bias to reach −5.4 V; (d) total instantaneous voltage across the diode; (e) a negative dc bias builds up across the gate-to-source.
The same basic circuit action occurs when gate leak bias is used. The situation is slightly more involved since the feedback signal rides on a 15-V dc level [see Fig. 15-19(e)]. A peak feedback signal of 3 V causes the total instantaneous feedback signal to go from 12 V up to 18 V. Consequently, the capacitor will charge to 17.4 V. As the oscillations build up, the average gate-to-source bias will reach -2.4 V.

The negative gate-to-source bias will lower the transconductance of the JFET. Consequently, the voltage gain and loop gain will be reduced. The output voltage signal will be very "clean." The forward bias on the gate will cause a drastic amount of distortion in the JFET's drain current. However, the high-Q tuned filter circuit will remove all of the "nasty" harmonics. The reduction in the duration of the flow of the drain current causes the voltage amplifier to leave class A operation and enter class B or even class C operation. Consequently, its efficiency is also increased (refer to Chapter 12).

The RFC \((L_2)\) should have an impedance that is much larger than the capacitive reactance of \(C_1\). A comfortable factor is 100:1. Hence

\[ X_{L_2} > 100X_{C_1} \]

The capacitive reactance of decoupling capacitor \(C_4\) should be small compared to \(X_{L_2}\). Again, a ratio of at least 100:1 is desirable. This would place the value of the decoupling capacitor at approximately that of \(C_1\). However, it is often selected to be much larger in practice.

**EXAMPLE 15-8**

Analyze the JFET Colpitts oscillator given in Fig. 15-17(b). Specifically, determine the frequency of oscillation \(f_o\), the minimum required open-circuit voltage gain, the actual voltage gain when power is first applied, and verify the proper sizing of \(L_2\) and \(C_4\).

**SOLUTION** From Eq. 15-37,

\[
C_T = \frac{C_1C_2}{C_1 + C_2} = \frac{(330 \text{ pF})(680 \text{ pF})}{330 \text{ pF} + 680 \text{ pF}} = 222.2 \text{ pF}
\]

\[
f_o = \frac{1}{2\pi\sqrt{LC_T}} = \frac{1}{2\pi\sqrt{(110 \mu\text{H})(222.2 \text{ pF})}} = 1.02 \text{ MHz}
\]

The minimum required open-circuit voltage gain may be determined using Eq. 15-38.

\[
A_{(\infty)} \leq \frac{C_2}{C_1} = -\frac{680 \text{ pF}}{330 \text{ pF}} = -2.06
\]

If we examine the data sheet for the 2N5458 n-channel JFET, we find that its minimum transconductance \(g_{f0}(\text{min})\) \((g_m)\) is 1500 \(\mu\text{S}\), and the magnitude of its drain-to-source admittance \(|y_{osl}(\text{max})|\) is 50 \(\mu\text{S}\) (at 1 kHz). This information will allow us to estimate the 2N5458's performance.

\[
A_{(\infty)} = -g_{f0}f_o = -g_{f0} \frac{1}{|y_{osl}|} = -(1500 \mu\text{S}) \left(\frac{1}{50 \mu\text{S}}\right) = -30
\]
The minimum voltage gain of the 2N5458 JFET is more than adequate in this circuit. Now let us investigate the gate leak bias circuit. When capacitor \( C_3 \) discharges, its discharge path is through \( R_G \). (The gate-to-source \( p-n \) junction is reverse biased.) For proper operation to occur, the discharge time constant should be at least 10 times longer than the period of the frequency of oscillation. Thus

\[
\tau = R_G C_3 = (100 \, \text{k}\Omega)(180 \, \text{pF}) = 18 \, \mu\text{s}
\]

and

\[
T = \frac{1}{f_o} = \frac{1}{1.02 \, \text{MHz}} = 0.980 \, \mu\text{s}
\]

Since

\[ \tau \geq 10 T \]

\[ 18 \, \mu\text{s} \geq (10)(0.980 \, \mu\text{s}) = 9.80 \, \mu\text{s} \]

the time constant appears to be better than required, and \( C_3 \) is adequately sized.

Now we shall check the values of the decoupling components \( L_2 \) and \( C_4 \). At \( f_o \),

\[
X_{C1} = \frac{1}{2\pi f_o C_1} = \frac{1}{2\pi(1.02 \, \text{MHz})(330 \, \text{pF})} = 473 \, \Omega
\]

The inductive reactance of the RFC is

\[
X_{L2} = 2\pi f_o L_2 = 2\pi(1.02 \, \text{MHz})(8.2 \, \text{mH}) = 52.6 \, \text{k}\Omega
\]

Hence

\[
X_{L2} \geq 100X_{C1}
\]

\[ 52.6 \, \text{k}\Omega \geq (100)(473 \, \Omega) = 47.3 \, \text{k}\Omega \]

Therefore, the RFC appears to have enough inductance. Since the decoupling capacitor \( C_4 \) is much larger than \( C_1 \), its capacitive reactance will certainly be small compared to \( X_{L2} \). Therefore, \( C_4 \) is adequately sized.

As a final comment, we should point out that the Colpitts oscillator given in Fig. 15-17(b) worked very well in the laboratory. The actual drain-to-ground and gate-to-ground waveforms have been illustrated in Fig. 15-17(b). Observe that the positive peak drain voltage is 11 V above \( V_{DD} \). This is typical of transistor circuits that have an inductive load. The ac load line indicates that the maximum value is equal to twice \( V_{DD} \).

15-12 Clapp Oscillators

The Clapp oscillator is a variation of the Colpitts oscillator. The single inductor found in the Colpitts oscillator is replaced by a series \( LC \) combination [see \( L_1 \) and \( C_3 \) in Fig. 15-20(a)]. At the frequency of oscillation the net impedance of the \( LC \) series network will be inductive.

The three impedances \( Z_1 \), \( Z_2 \), and \( Z_3 \) have been indicated in Fig. 15-20(a). A more conventional schematic has been depicted in Fig. 15-20(b). Also note that actual measured waveforms have also been indicated. Let us again develop our equations for \( f_o \) and the minimum \( A_{v(\infty)} \).
FIGURE 15-20 Clapp oscillator: (a) basic Clapp oscillator; (b) practical oscillator; (c) the JFET's $C_m$ is in parallel with $C_2$, and the JFET's $C_{out}$ is in parallel with $C_1$. 
At resonance we recall that
\[ Z_1 + Z_2 + Z_3 = 0 \]
Substituting in the specific impedance, we have
\[ -j \frac{1}{\omega_0 C_1} - j \frac{1}{\omega_0 C_2} - j \frac{1}{\omega_0 C_3} + j \omega_0 L_1 = 0 \]
\[ j \omega_0 L_1 = j \frac{1}{\omega_0} \left( \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \right) \]
The terms on the right side of the equation represent the series combination of \( C_1 \), \( C_2 \), and \( C_3 \). Hence
\[ \frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \]
Substituting in this standard relationship for capacitors in series leads us to
\[ \omega_0^2 = \frac{1}{L_1 C_T} \]
\[ f_o = \frac{1}{2\pi \sqrt{L_1 C_T}} \tag{15-39} \]
where \( f_o \) = Clapp oscillator frequency of oscillation (hertz)
\( L_1 \) = feedback inductance
\( 1/C_T \) = reciprocal of the series equivalent capacitance = \( 1/C_1 + 1/C_2 + 1/C_3 \)

The minimum open-circuit voltage gain required to guarantee oscillation is given by Eq. 15-40. It is derived in exactly the same fashion as Eq. 15-38 for the Colpitts oscillator.

\[ A_{v(oc)} < -\frac{C_2}{C_1} \tag{15-40} \]
where \( A_{v(oc)} \) is the open-circuit voltage gain of the amplifier used in the Clapp oscillator.

Let us reflect on these results. The addition of capacitor \( C_3 \) lowers the total equivalent capacitance \( C_T \). Consequently, the values of capacitors \( C_1 \) and \( C_2 \) can be increased and still produce a relatively small \( C_T \). This advantage becomes more apparent when we look at Fig. 15-20(c).

The total input capacitance of the JFET (\( C_m \)) is in parallel with \( C_2 \), and the JFET's output capacitance (\( C_{os} \)) is in parallel with \( C_1 \). This increases the net "\( C_1 \)" capacitance, and the net "\( C_2 \)" capacitance. Therefore, these small device capacitances tend to lower the frequency of oscillation. To compound the problem, the JFET capacitances are not very tightly controlled parameters and are affected by the dc bias. This introduces a measure of uncertainty in the oscillator design. The situation becomes particularly acute when the oscillator is to be used at very high frequencies (e.g., above 10 MHz) since the values of \( C_1 \) and \( C_2 \) tend to be small.

Therefore, the fact that we are able to increase the values of \( C_1 \) and \( C_2 \)(and
still obtain a small $C_T$) tends to negate this effect. The device capacitances can be "swamped out."

Typically, capacitor $C_3$ is selected to be the smallest capacitor. This makes it dominate in the determination of $f_o$. However, caution must be exercised. If capacitor $C_3$ is made too small, the $LC$ branch will not have a net inductive reactance. Under this condition the circuit will refuse to oscillate.

Capacitors $C_1$ and $C_2$ [Fig. 15-20(b)] are approximately twice the values given for $C_1$ and $C_2$ in Fig. 15-17(b). Capacitor $C_3$ is the smallest and approximately equal to the series combination of $C_1$ and $C_2$ in Fig. 15-20(b). Therefore, the net $C_T$ of the Clapp oscillator is approximately equal to the $C_T$ of the Colpitts oscillator. Since the inductance $L_1$ is still 110 $\mu$H, the frequency of oscillation of the Clapp oscillator will be approximately equal to that of the Colpitts oscillator given in Fig. 15-17(b). The next example will verify this.

### EXAMPLE 15-9

Determine $f_o$, the minimum open-circuit voltage gain, and the net impedance of the $L_1$-$C_3$ branch at $f_o$ of the Clapp oscillator given in Fig. 15-20(b).

#### SOLUTION

The frequency of oscillation may be found by using Eq. 15-39.

$$
C_T = \frac{1}{1/C_1 + 1/C_2 + 1/C_3} = \frac{1}{1/680 \text{ pF} + 1/1500 \text{ pF} + 1/390 \text{ pF}} = 212.7 \text{ pF}
$$

$$
f_o = \frac{1}{2\pi \sqrt{L_1 C_T}} = \frac{1}{2\pi \sqrt{(110 \mu \text{H})(212.7 \text{ pF})}} = 1.04 \text{ MHz}
$$

The minimum open-circuit voltage gain is given by Eq. 15-40.

$$
A_v(\text{oc}) \leq -\frac{C_3}{C_1} = -\frac{1500 \text{ pF}}{680 \text{ pF}} = -2.21
$$

Now we can determine the net impedance of the $L_1$-$C_3$ branch.

$$
Z_{net} = jX_{L_1} - jX_{C_3} = j2\pi f_o L_1 - j\frac{1}{2\pi f_o C_3}
$$

$$
= j2\pi (1.04 \text{ MHz})(110 \mu \text{H}) - j\frac{1}{2\pi (1.04 \text{ MHz})(390 \text{ pF})}
$$

$$
= j719.1 \Omega - j392.2 \Omega = j326.9 \Omega
$$

The rest of the analysis of the Clapp oscillator is identical to that conducted on the Colpitts oscillator covered in Example 15-8. Specifically, the JFET's $A_v(\text{oc})$ is more than adequate, the gate leak bias time constant is acceptable, and the decoupling action of $L_2$ and $C_3$ exceeds the minimum requirements.

### 15-13 Hartley Oscillators

The Hartley oscillator is almost as popular as the Colpitts oscillator. It may be thought of as the "complement" of the Colpitts oscillator. Specifically, the Colpitt's inductor is replaced by a capacitor, and the two capacitors found in Colpitt's feedback network...
are replaced by inductors (refer to Table 15-2). The basic Hartley configuration has been depicted in Fig. 15-21(a).

Two separate inductors are seldom employed in "real" Hartley oscillators. Instead, most designs incorporate a single tapped inductor [see Fig. 15-21(b)]. A tapped inductor with a single winding will behave as an autotransformer. An autotransformer employs a single winding. Consequently, it offers no isolation, but it can be used to either step up or step down a voltage signal [see Fig. 15-21(c) - (e)]. As we shall see, the transformer action will determine the feedback factor (β) of the oscillator. The phasing of the transformer with respect to ground is also configured to provide positive feedback.

**FIGURE 15-21** Hartley oscillator using a tapped inductor: (a) two separate inductors; (b) using a single tapped inductor; (c) step-down autotransformer; (d) step-up autotransformer; (e) step-up or step-down with phase inversion.
Since the tapped inductor is crucial to proper operation of the Hartley oscillator, it merits additional attention. A single-layer, air-core coil has been illustrated in Fig. 15-22(a). The inductance of the coil is dependent on its geometry and is directly proportional to the square of its turns.

\[
L = \frac{r^2N^2}{9r + 10l}
\]  
(15-41)

where \( L \) = inductance (microhenries)  
\( r \) = mean radius of the coil (inches)  
\( N \) = number of turns  
\( l \) = length of the coil (inches)

From a design standpoint, we are interested in solving for the required number of turns \((N)\). This is accomplished by solving Eq. 15-41 for \( N \).

\[
N = \sqrt{\frac{L(9r + 10l)}{r^2}}
\]  
(15-42)

Equations 15-41 and 15-42 are approximations. They do not take into account variables such as uneven turns and unequal spacing between the turns. Therefore, they serve only to give us a rough estimate.
EXAMPLE 15-10

A single-layer air-core inductor is to be used in a Hartley oscillator. It is to have 100 $\mu$H of inductance and be wound on a 2-W carbon resistor. Complete its design.

**SOLUTION** A 2-W resistor has a length of 0.688 in. and a diameter of 0.312 in. Its radius is one-half of its diameter.

$$r = \frac{d}{2} = \frac{0.312 \text{ in.}}{2} = 0.156 \text{ in.}$$

and since its length ($l$) is 0.688 in., we can use Eq. 15-42 to determine the required number of turns ($N$).

$$N = \sqrt{\frac{L(9r + 10)}{r^2}} = \sqrt{\frac{100(9(0.156) + 10(0.688))}{(0.156)^2}}$$

$$= 184.5 \approx 184 \text{ turns}$$

Observe that we have rounded our answer to the nearest turn. Now we can determine the wire size. The wire diameter $D$ is

$$D = \frac{1}{N} \frac{0.688 \text{ in.}}{184} = 0.00374 \text{ in.}$$

Going to a wire table we find that 39 AWG (American Wire Gauge) enameled copper wire has a nominal diameter of 0.00353 in. The wire has a resistance of 0.832 m$\Omega$/ft. The circumference ($c$) of the 2-W resistor is

$$c = \pi d = \pi (0.312 \text{ in.}) = 0.980 \text{ in.}$$

Now we can determine the required length of 39 AWG wire.

wire length = $Nc = (184)(0.980 \text{ in.}) = 180.3 \text{ in.} = 15.0 \text{ ft}$

The total dc resistance of the wire used to make the coil is

$$R_{dc} = (0.832 \text{ m$\Omega$/ft})(15.0 \text{ ft}) = 0.0125 \Omega$$

Such a small dc resistance will promote a high-$Q$ coil. (Remember that ac losses will also come into play, but these are not easily predicted.)

EXAMPLE 15-11

The coil designed in Example 15-10 is to be tapped such that

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} = \frac{1}{3}$$

[refer to Fig. 15-21(e)]. At present we ignore the phase inversion.

**SOLUTION** We shall solve for $N_2$. First, we apply the relationship above.

$$N_2 = \frac{1}{3}N_1$$

By inspection of Fig. 15-21(e),

$$N = N_1 + N_2$$

and solving for $N_1$ gives us

$$N_1 = N - N_2$$

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If we substitute this result into the previous relationship, we can solve for $N_2$.

$$N_2 = \frac{1}{4}N_1 = \frac{1}{4}(N - N_2) = \frac{1}{4}N - \frac{1}{4}N_2$$

$$\frac{1}{4}N_2 = \frac{1}{4}N$$

$$N_2 = \frac{1}{4}N = \left(\frac{1}{4}\right)(184 \text{ turns}) = 46 \text{ turns}$$

The complete inductor has been shown in Fig. 15-22(b). The resistor is 750 kΩ. Its large resistance will have a negligible shunting effect on our coil. We shall use this inductor in our examples to come.

A Hartley oscillator that employs a common-source JFET has been indicated in Fig. 15-23(a). Notice that the tapped inductor ($L_1$) designed in Examples 15-10.

**FIGURE 15-23** Operation of the JFET Hartley oscillator: (a) JFET Hartley oscillator; (b) transformer action of the tapped inductor; (c) partial ac equivalent.
and 15-11 has been incorporated in its resonant circuit. The autotransformer action
of \( L_1 \) has been emphasized in Fig. 15-23(b). By inspection we see that

\[
\beta = \frac{V_L}{V_{out}} = \frac{N_2}{N_1} = -\frac{46 \text{ turns}}{139 \text{ turns}} = -0.331
\]

The step-down action of the inductor provides a \( \beta \) that is less than unity. The
negative sign indicates that the transformer provides 180° of phase shift [see Fig.\n15-23(c)].

The JFET provides an open-circuit voltage gain of

\[
A_{v(oc)} = -g_m r_o = -g_{fd} r_o
\]

From our work in Example 15-8 we recall that the \( A_{v(oc)} \) for the 2N5458 JFET is
-30. Consequently, the loop gain is (approximately)

\[
\beta A_{v(oc)} = (-0.331)(-30) = 9.93 > 1
\]

Therefore, the circuit will oscillate. The approximation above has drawn on the open-
circuit voltage gain. To be rigorous, we should use the loaded voltage gain. Some
impedance will be reflected back into the primary of our autotransformer, and this
reflected impedance will load down the amplifier's output. However, this effect can
be ignored except in critical applications.

Now let us determine the frequency of oscillation. It is given by the resonant
frequency of the \( L_1 C_1 \) combination.

\[
f_o = \frac{1}{2\pi \sqrt{L_1 C_1}} = \frac{1}{2\pi \sqrt{(100 \mu F)(240 \mu F)}} = 1.03 \text{ MHz}
\]

The balance of the circuit's operation - the gate leak bias and the decoupling
action afforded through the use of \( L_2 \) and \( C_4 \) - has been examined previously. Now
let us consider a common-emitter Hartley oscillator [see Fig. 15-24(a)].

Although more components are involved in this design, its operation will become
clear if we do not panic. Capacitor \( C_4 \) is a decoupling capacitor. Capacitors \( C_2 \) and
\( C_3 \) are used to block the dc biases. They are shorts to the ac signal. Capacitor \( C_3 \) is
an emitter bypass capacitor. A partial ac equivalent circuit has been depicted in Fig.
15-24(b).

Once we recognize that \( L_2 \) is an RFC, we may redraw the circuit as shown in
Fig. 15-24(c). At this point it should be clear that the analysis of the circuit is virtually
identical to the JFET Hartley oscillator given in Fig. 15-23(a).

We conclude our discussions of the Hartley oscillator with the circuit given in
Fig. 15-25(a). The circuit is novel in that it is designed around an emitter follower.
The less than unity voltage gain offered by the emitter follower would seem to prohibit
oscillations. However, this is not the case. The loop gain can be made greater than
unity because of the step-up transformer action produced by \( L_1 \).

The base bias circuit is designed to offer good bias stability, provide power
supply decoupling, and simultaneously present a relatively large equivalent resistance
to the tank circuit. Let us perform a dc analysis. The oscillator's dc equivalent circuit
has been indicated in Fig. 15-25(b).
EXAMPLE 15-12

Determine the dc collector current of $Q_1$ in Fig. 15-25(a). Also determine the voltage drop across $R_3$.

SOLUTION First, we Thévenize the base circuit as indicated in Fig. 15-25(b).

$R_{TH} = R_1 \| R_2 + R_3 = 3.3 \text{k}\Omega \| 3.3 \text{k}\Omega + 20 \text{k}\Omega = 21.65 \text{k}\Omega$  

$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{3.3 \text{k}\Omega}{3.3 \text{k}\Omega + 3.3 \text{k}\Omega} (15 \text{ V}) = 7.5 \text{ V}$
FIGURE 15-25  Hartley oscillator using an emitter follower: (a) complete circuit; (b) dc equivalent; (c) partial ac equivalent.
Now we can determine $I_B$. The 2N4124 has a minimum $h_{FE}$ of 120.

\[
I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1 + h_{FE})R_4} = \frac{7.5 \text{ V} - 0.7 \text{ V}}{21.65 \text{ k}\Omega + (1 + 120)(6.8 \text{ k}\Omega)} = 8.05 \text{ \mu A}
\]

Now we can find $I_C$.

\[
I_C = h_{FE}I_B = (120)(8.05 \text{ \mu A}) = 0.966 \text{ mA}
\]

The voltage drop across $R_3$ is very small.

\[
V_{R3} = I_BR_3 = (8.05 \text{ \mu A})(20 \text{ k}\Omega) = 0.161 \text{ V}
\]

\[\square\]

EXAMPLE 15-13

Determine the open-circuit voltage gain of the emitter follower in Fig. 15-25(a).

**SOLUTION** First, we must determine the BJT's $g_m$.

\[
g_m = \frac{I_C}{26 \text{ mV}} = \frac{0.966 \text{ mA}}{26 \text{ mV}} = 32.2 \text{ mS}
\]

Now we can find $A_{v(oc)}$.

\[
A_{v(oc)} = \frac{g_mR_4}{1 + g_mR_4} = \frac{(37.2 \text{ mS})(6.8 \text{ k}\Omega)}{1 + (37.2 \text{ mS})(6.8 \text{ k}\Omega)} = 0.996
\]

\[\square\]

A partial ac equivalent circuit has been given in Fig. 15-25(c). The output voltage of the emitter follower has been impressed across the 'N1' turns of the tapped inductor. However, the feedback voltage is taken across the entire coil. This will produce step-up (N/N2) transformer action. Therefore, the $\beta$ will be greater than unity.

\[
\beta = \frac{N}{N_2} = \frac{184 \text{ turns}}{46 \text{ turns}} = 4
\]

Notice that in this scheme there is no phase inversion. Consequently, $\beta$ is positive, and the loop gain is

\[
\beta A_v = \frac{N}{N_2} A_{v(oc)} = (4)(0.996) = 3.98 > 1
\]

and the circuit will oscillate. [Notice that we have again used $A_{v(oc)}$ as an approximation of $A_v$.]

The frequency of oscillation is determined by $L_1$ and $C_1$. From our analysis of the common-source JFET circuit we recall that with an $L_1$ of 100 $\mu$H and a $C_1$ of 240 pF, $f_0$ occurs at 1.03 MHz. The same formula is used.

15-14 The Crystal

Some crystalline materials, such as quartz, tourmaline, and Rochelle salts, demonstrate a property called the piezoelectric effect. Very simply, if they are mechanically forced to vibrate, the resulting strain produces an electrical charge on the surface of the crystal and it generates an ac voltage. Conversely, if they are excited by an ac voltage, they will vibrate mechanically. Both modes of operation are commonly used.
In transducer applications the crystal is used to convert mechanical energy into electrical energy. Examples include crystal microphones, dynamic pressure transducers, and accelerometers.

The vibration of a crystal [Fig. 15-26(a) and (b)] that is excited by an ac voltage is capitalized on in RF electrical filters and in the tuned circuits of oscillators. As the frequency of a crystal’s excitation voltage is changed, its response to the signal will change. The electrical properties of a piezoelectric crystal are quite dramatic when it enters mechanical resonance. For our purposes, we utilize the crystal’s electrical equivalent circuit given in Fig. 15-26(c). Capacitance $C_m$ represents the static capacitance produced by the contact wires, the crystal electrodes, and the crystal holder. The series $RLC$ combination represents the motional aspects of the crystal. Capacitance $C_s$ models the mechanical elasticity, the inductance $L_s$ is a function of the crystal’s mass, and $R_s$ includes all the mechanical and electrical losses in the crystal.

**FIGURE 15-26** Crystal: (a) typical crystal package; (b) schematic symbol; (c) electrical equivalent circuit; (d) impedance and phase angle versus frequency.
Quartz is the most often selected material. The fundamental resonant frequencies for quartz typically range from 0.8 kHz to 50 MHz. Higher (up to 250 MHz) resonant frequencies are also available. The higher resonant frequencies are made possible by constructing crystals to operate at multiples (overtones) of their fundamental frequency. The third, fifth, and seventh overtones are the most commonly used.

Approximate values in the equivalent circuit of a particular 2-MHz crystal are a $C_s$ of 0.012 pF, an $L_s$ of 0.5 H, an $R_s$ of 100 $\Omega$, and a $C_m$ of 4 pF. Crystals can offer extremely high $Q$’s - values exceeding 100,000 are not uncommon. The $Q$ of the 2-MHz crystal described above is given as 64,550.

The impedance of a crystal as a function of frequency has been shown in Fig. 15-26(d). At low frequencies the capacitive reactance of $C_s$ dominates. As the frequency is increased to $f_s$, the crystal will go into series resonance. This occurs when the magnitude of $X_{C_s}$ is equal to the magnitude of $X_{L_s}$. The net impedance of the crystal is resistive, and equal to $R_s$.

As the frequency is increased beyond $f_s$, $X_{L_s}$ will "swamp out" $X_{C_s}$, and the crystal’s net impedance will be inductive. If the frequency is increased to $f_p$, the crystal enters its parallel resonant mode of operation. At $f_p$, the net inductive susceptance of the $RLC$ branch equals the capacitive susceptance of $C_m$. The crystal’s impedance will be extremely large. At frequencies beyond $f_p$, the crystal’s impedance will again become capacitive. The capacitive susceptance of $C_m$ will dominate.

**EXAMPLE 15-14**

Determine the $f_s$, the impedance at $f_s$, the $Q$, the $f_p$, and the impedance at $f_p$ of a crystal with a $C_s$ of 0.0060 pF, an $L_s$ of 0.165609 H, an $R_s$ of 10 $\Omega$, and a $C_m$ of 13.0 pF.

**SOLUTION** The series resonant frequency is determined by $C_s$ and $L_s$. (The magnitude of their respective reactances will be equal.)

$$f_s = \frac{1}{2\pi \sqrt{L_s C_s}} = \frac{1}{2\pi \sqrt{(0.0060 \text{ pF})(0.165609 \text{ H})}}$$

$$= 5.048967 \text{ MHz}$$

The impedance of the crystal at series resonance is equal to $R_s$ (10 $\Omega$). Now we determine the $Q$.

$$X_{L_s} = 2\pi f_s L_s = 2\pi(5.048967 \text{ MHz})(0.165609 \text{ H})$$

$$= 5.253713 \text{ M$\Omega$}$$

$$Q = \frac{X_{L_s}}{R_s} = \frac{5.253713 \text{ M$\Omega$}}{10 \Omega} = 525.371$$

The parallel resonant frequency occurs when the equivalent parallel susceptance of the $RLC$ branch is equal to the magnitude of the capacitive susceptance of $C_m$. When the resonant network has a high $Q$, we may approximate the true condition by stating that the reactances will sum to zero. This requires us first to determine the equivalent series capacitance of $C_s$ and $C_m$.

$$\frac{1}{C_T} = \frac{1}{C_s} + \frac{1}{C_m} = \frac{1}{0.006 \text{ pF}} + \frac{1}{13 \text{ pF}} = 1.6674 \times 10^{14} \text{ F}^{-1}$$

$$C_T = 0.005997232 \text{ pF}$$

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\[ f_p = \frac{1}{2\pi \sqrt{L_s C_T}} = \frac{1}{2\pi \sqrt{(0.005997232 \text{ pF})(0.165609 \text{ H})}} = 5.050146 \text{ MHz} \]

The impedance of the crystal at parallel resonance may be determined by employing Eq. 15-30. However, we must first determine the net \( Q \) of the \( RLC \) branch. At \( f_p \), \( X_{L_s} \) is

\[ X_{L_s} = 2\pi f_p L_s = 5.254939 \text{ M}\Omega \]

and the capacitive reactance of \( C_s \) is

\[ X_{C_s} = \frac{1}{2\pi f_p C_s} = 5.252487 \text{ M}\Omega \]

At \( f_p \) the net impedance of the \( RLC \) branch will be inductive.

\[ X_{L(\text{net})} = X_{L_s} - X_{C_s} = 5.254939 \text{ M}\Omega - 5.252487 \text{ M}\Omega = 2.452 \text{ k}\Omega \]

The net \( Q \) can now be found.

\[ Q_{(\text{net})} = \frac{X_{L(\text{net})}}{R_s} = \frac{2.452 \text{ k}\Omega}{10 \text{ k}\Omega} = 245.2 \]

Now from Eq. 15-30,

\[ R_p = Q_{(\text{net})}^2 R_s = (245.2)^2(10 \Omega) = 601.2 \text{ k}\Omega \]

From Example 15-14 we can see that \( f_s \) occurs before \( f_p \). The frequency difference between the two is quite small (1.179 kHz). The impedance at series resonance is small (10 \( \Omega \)) and the parallel resonant impedance is much larger (approximately 601 k\( \Omega \)).

Quartz crystals are typically specified to operate in either their series or parallel resonant mode. For example, an M-tron MP-2 1-MHz crystal is intended to be used in parallel resonance with an equivalent load capacitance (\( C_{\text{load}} \)) of 18 pF across it. The crystal has a maximum \( R_s \) of 500 \( \Omega \) with typical values ranging from 100 to 125 \( \Omega \).

The load capacitance statement above is very important. It is possible to "pull," or shift the parallel resonant operating frequency (\( f_{\text{op}} \)) of a crystal by changing its load capacitance. The load capacitance is in parallel with the mounting capacitance \( C_m \) (see Fig. 15-27).

The equivalent capacitance in Fig. 15-27(a) is the parallel combination of \( C_m \) and \( C_{\text{load}} \) in series with \( C_s \). Therefore, the crystal's operating frequency is given by

\[ f_{\text{op}} = \frac{1}{2\pi \sqrt{L_s \left( C_s \left( C_m + C_{\text{load}} \right) \left/ \left( C_s + \left( C_m + C_{\text{load}} \right) \right) \right) \right)}} \]  

(15-43)

where \( f_{\text{op}} \) is the parallel resonant frequency of a crystal with an external load capacitance. The \( f_{\text{op}} \) of a crystal lies between \( f_s \) and \( f_p \). With no load capacitance (a \( C_{\text{load}} \) of zero) \( f_{\text{op}} \) will be equal to \( f_p \). As \( C_{\text{load}} \) becomes larger, \( f_{\text{op}} \) will approach \( f_s \). In practice,

\[ f_s < f_{\text{op}} < f_p \]

(15-44)

[see Fig. 15-27(b)].
FIGURE 15-27 Crystals designed to operate in their parallel resonant mode have a specified load capacitance: (a) the circuit's parallel resonant (operating) frequency is \( f_{op} \); (b) the \( C_{load} \) pulls the parallel resonant frequency toward the series resonant frequency.

### EXAMPLE 15-15

Determine the operating frequency \( f_{op} \) of the crystal analyzed in Example 15-14 if \( C_{load} \) is 12 pF.

**SOLUTION** Using the data given in Example 15-14 and Eq. 15-43, we can determine the crystal's operating frequency.

\[
\begin{align*}
 f_{op} &= \frac{1}{2\pi \sqrt{L_{s}\left[C_{s}(C_{m} + C_{load})/(C_{s} + (C_{m} + C_{load}))\right]}} \\
 &= \frac{1}{2\pi \sqrt{(0.165609 \, \text{H})\left[\frac{(0.006 \, \text{pF})(13 \, \text{pF} + 12 \, \text{pF})}{[0.006 \, \text{pF} + (13 \, \text{pF} + 12 \, \text{pF})]\}} \\
 &= 5.049573 \, \text{MHz}
\end{align*}
\]

If we compare \( f_{op} \) with \( f_{p} \), we see that \( C_{load} \) has lowered the crystal's parallel resonant frequency. Parallel resonance is now only about 606 Hz above the crystal's series resonant frequency. The effect of \( C_{load} \) on \( f_{op} \) has been illustrated in Fig. 15-28(a). The significance of \( f_{op} \) in oscillator circuits will be demonstrated in the next section.

From our previous work it should be clear that the phase shift across the frequency-determining feedback network in oscillator circuits is critical. When an inverting amplifier is used, the ac feedback is intended to provide about 180° of phase
FIGURE 15.28 Crystal parameters: (a) effect of $C_{\text{load}}$ on $f_{\text{op}}$; (b) typical temperature characteristic curve.

shift at the desired frequency of oscillation ($f_{\text{op}}$). If the $Q$ of the feedback network is low, the change in the phase shift with frequency is gradual. Therefore, the frequency of oscillation is free to "wander" or drift over a relatively wide range of values. A stable oscillator demands a high-$Q$ feedback network. A high-$Q$ network maximizes the change in phase shift with frequency.

If we turn back to Fig. 15.26(d), we see that the phase shift offered by a crystal abruptly changes on either side of $f_s$ and $f_p$. This occurs because of its inherently large $Q$. With this in mind it should be clear why crystal-based oscillator designs can offer excellent frequency stability.

The resonant frequency of an oscillator's tuned circuit is also critical. In the case of a discrete $LC$ resonant circuit, the temperature coefficient of the capacitors and inductors come into play. Capacitors are available which have positive, negative, and zero temperature coefficients. Coils, however, generally only have positive temperature coefficients. Making a tuned circuit that is insensitive to temperature is a difficult endeavor. To keep the $LC$ product constant, the capacitor's tempco must be negative to compensate for the inductor's positive tempco. The tempcos must be matched, and the components should be thermally bonded together.

The resonant frequency of a crystal also changes with temperature. However, it is much more predictable. A typical temperature curve has been depicted in Fig. 15.28(b). The turning point is the temperature at which the crystal's deviation from resonance is zero. For temperatures below the turning point, the crystal's resonant frequency will increase. For temperatures above the turning point, the crystal's resonant frequency will be decreased. We should emphasize that Fig. 15.28(b) shows the general shape of a temperature characteristic. If specific questions arise about a particular crystal, its manufacturer should be consulted. In demanding applications,
it is not unusual to find the crystal housed in a small oven. The oven is typically used to regulate the crystal’s temperature at its turning-point value.

The unit “ppm” in Fig. 15-28(b) stands for “parts per million.” For example, if a 5-MHz crystal’s resonant frequency has increased 20 ppm, the change in frequency (Δf) is

\[ Δf = (5 \times 10^6 \text{ Hz})(20 \times 10^{-6}) = 100 \text{ Hz} \]

The use of ppm units is quite extensive in the electronics industry and not just associated with crystals.

15-15 Crystal Oscillators

As we mentioned in Section 15-14, the extremely high \( Q \) of a crystal can be used to produce oscillators with excellent frequency stability. In practice, a crystal may be used to replace an entire \( LC \) resonant network, or it may be used to replace one or more of the reactances normally found in such a network. We shall see examples of these alternatives in our work to follow.

In Fig. 15-29(a) we see a general form of the Pierce crystal oscillator. In essence, it is a Clapp oscillator in which the inductor and its small series capacitance are replaced by a quartz crystal. The very small \( C_s \) of the crystal dominates. The crystal is typically operated slightly above its series resonant frequency \( f_s \). Therefore, the net impedance of the crystal is a resistance in series with an inductive reactance. The crystal’s equivalent circuit has been emphasized in Fig. 15-29(a). The Pierce oscillator is one of the most popular crystal oscillator circuits.

We see a practical Pierce oscillator circuit in Fig. 15-29(b). At first glance, most students will not immediately recognize that the circuit is in the configuration indicated in Fig. 15-29(a). This is because the output (device) capacitance of the JFET is used as the “\( C_1 \)” of the feedback network, and the JFET’s input capacitance is used as the “\( C_2 \)” This is indicated in Fig. 15-29(c).

The small \( C_1 \) and \( C_2 \) capacitances produce relatively large capacitive reactances. Therefore, the inductive reactance of the crystal is also large, and it operates considerably above series resonance. Observe that an M-tron MP-2 crystal has been indicated. As we mentioned in Section 15-14, this crystal is intended to operate in the parallel resonant mode. Laboratory work indicated that the circuit in Fig. 15-29(b) operates at a frequency of 999.997 kHz. This is 3 Hz below the crystal’s nominal parallel resonant frequency of 1.000 MHz, and 197 Hz above the crystal’s series resonant frequency of 999.800 kHz.

Obviously, the crystal oscillator given in Fig. 15-29(b) requires a minimal number of components. However, the addition of a small adjustable capacitor (called a “trimmer”) from the gate of the JFET to ground allows the output frequency to be adjusted. As the capacitance of the trimmer is increased, the frequency of oscillation will be lowered. The additional capacitance will pull the crystal’s operating frequency toward series resonance.

In Fig. 15-30(a) we see an improved Pierce oscillator circuit. Specifically, capacitors \( C_1 \) and \( C_2 \) have been added to “swamp out” the JFET’s input and output device capacitances. While using the JFET’s capacitances to minimize the component
count results in a simple circuit, it can also open the door to problems if the circuit enters mass production. Manufacturers will generally limit the maximum values of the device capacitances, but they are not otherwise tightly controlled parameters. Consequently, the mass production of such circuits could lead to a production run of oscillators that refuse to oscillate, or whose frequency is out of tolerance. The use of capacitors $C_1$ and $C_2$ tends to minimize this problem.

Capacitor $C_3$ has been added to provide gate leak bias. This serves to minimize the distortion in the oscillator's output waveform.

The increased capacitance ($C_1$, $C_2$, and $C_3$) across the crystal pulls its operating frequency much closer to series resonance. In a "good" Pierce oscillator design, the net impedance of the crystal is only slightly inductive. Typically, the crystal will operate 10 to 50 ppm above series resonance.
FIGURE 15-30  Improved Pierce oscillator and its ideal analysis:
(a) when capacitances $C_1$ and $C_2$ are added the crystal operates much closer to its series resonant frequency; (b) Ideal equivalent circuit $- R_s \ll X_{Ls(net)}$; (c) the amplifier's output drives an ideal parallel resonant circuit; (d) the feedback factor has a magnitude of $C_1/C_2$ and provides $-180^\circ$ of phase shift.
In Fig. 15-30(a) we see actual laboratory measurements. The output frequency was 999.850 kHz. This was 50 Hz above the crystal's series resonant frequency of 999.800 kHz.

From our previous work, we recall that the main thrust of any oscillator analysis lies in the determination of its feedback factor \( \beta \). This problem is particularly unwieldy in crystal oscillators. In our previous work we assumed that the inductor's resistance was negligibly small. This greatly simplified our work and resulted in very reasonable approximations. In "real" Pierce oscillators, this is unfortunately not the case. The crystal's internal resistance \( R_s \) is significant.

To understand the effect of \( R_s \), let us first review the ideal analysis from a slightly different perspective (refer to Fig. 15-30(b)). As we can see, we have again assumed that the amplifier's input impedance \( Z_{in} \) is large enough to be ignored. Hence

\[
Z_{in} \gg X_{C2}
\]

We have also assumed that \( R_s \) is negligibly small. Observe that the net inductive reactance \( X_{L_{net}} \) is in series with \( X_{C2} \). Also note that we have assumed that the sum of the three reactances is zero at resonance.

\[
+jX_{L_{net}} - jX_{C1} - jX_{C2} = 0
\]

Therefore, we may state that

\[
X_{L_{net}} = X_{C1} + X_{C2}
\]

Now we shall solve for the \( \beta \) of this idealized network. First, we find its loading effect on the amplifier's output. The series combination of \( X_{L_{net}} \) and \( X_{C2} \) produces

\[
+jX_{L_{net}} - jX_{C2} = (jX_{C1} + jX_{C2}) - jX_{C2} = jX_{C1}
\]

The positive equivalent impedance \( jX_{C1} \) is in parallel with capacitor \( C_1 \) \((-jX_{C1})\) [see Fig. 15-30(c)]. The output of the amplifier therefore drives a parallel resonant circuit. Ideally, a parallel resonant circuit acts like an open circuit. Therefore, the output of the amplifier is effectively unloaded. This means that the amplifier's output impedance \( Z_{out} \) has no effect on the \( \beta \) of the feedback network, and \( V_{out} \) appears across capacitor \( C_1 \) [see Fig. 15-30(d)].

Voltage division between the inductive reactance and \( X_{C2} \) determines the feedback factor \( \beta \). Hence

\[
\beta = \frac{V_i}{V_{out}} = \frac{-jX_{C2}}{jX_{C1} + jX_{C2} - jX_{C1}} = \frac{-jX_{C2}}{+jX_{C1}} = \frac{1/\omega_s C_2 \angle -90^\circ}{1/\omega_s C_1 \angle +90^\circ} = \frac{\omega_s C_1}{\omega_s C_2} \angle +90^\circ \angle -180^\circ = \frac{1}{C_2} \angle -180^\circ = -\frac{C_1}{C_2}
\]

This is the same relationship that we previously determined for both the Colpitts and Clapp oscillators.

The feedback network has given us a gain of \( C_1/C_2 \) and provides \( 180^\circ \) of phase shift. Therefore,

\[
A_{\phi_{in}} < -\frac{C_2}{C_1}
\]
to provide a loop gain with $0^\circ$ of phase shift and a magnitude greater than unity. Now let us consider the case where $R_r$ is not negligibly small [see Fig. 15-31(a)].

The following four points apply to "real" Pierce crystal oscillators:

1. The sum of the reactances must be equal to zero to provide $180^\circ$ of phase shift across the frequency-determining feedback network.

$$-jX_{C1} - jX_{C2} + jX_{L} = 0,$$

**FIGURE 15-31** More accurate analysis of the Pierce oscillator: (a) the crystal's equivalent series resistance is significant and the sum of the three reactances is zero; (b) approximation of the load across the amplifier's output; (c) determination of the feedback factor $\beta$.
and therefore

\[ jX_L = jX_{C1} + jX_{C2} \]

This statement allows us to determine the net inductive reactance of the crystal as it operates above series resonance.

2. Most designs set the capacitive reactance of \( C_2 \) to be much less than the \( Z_{in} \) of the amplifier. Therefore, we will assume that

\[ X_{C2} << Z_{in} \]

This statement allows us to ignore \( Z_{in} \) and greatly simplifies the analysis.

3. The equivalent series resistance of the crystal \( (R_s) \) is significant when compared to the other impedance levels. This is an unfortunate fact of life. It is very important to consider \( R_s \) in both the analysis and design of crystal oscillators. Fortunately, most crystal manufacturers include \( R_s \) on their data sheets.

4. Because \( R_s \) is significant, the output of the amplifier does not drive an ideal parallel resonant circuit. Therefore, the output impedance of the amplifier must be included in the analysis.

One approach to the analysis of the feedback network is to generate a single equation for the feedback factor \( \beta \). However, this results in a third-order equation, and the mathematics can quickly become overwhelming. To keep our sanity and to promote a more intuitive understanding, we shall break the analysis down into four relatively simple steps:

1. Find the load \( (Z_L) \) across the output of the amplifier.
2. Determine the gain from the amplifier's output to the feedback capacitor \( C_1 \) and call it \( \beta' \).
3. Find the gain from capacitor \( C_1 \) to capacitor \( C_2 \) and call it \( \beta'' \).
4. Multiply these two loaded gains (\( \beta' \) times \( \beta'' \)) to obtain the overall feedback factor \( \beta \).

The feedback circuit used in Fig. 15-30(a) has been redrawn in Fig. 15-31(a). The indicated reactances were determined at the oscillation frequency of 999.850 kHz. The reader should verify the values.

First, we shall find \( Z_L \) [refer to Fig. 15-31(b)]. By inspection we can see that the series combination of \( X_{L\text{load}} \), \( R_s \), and \( X_{C2} \) reduces to an equivalent inductive reactance \( (jX_{C1}) \) in series with \( R_s \). This series combination \( (Z'_L) \) is in parallel with \(-jX_{C1}\). Since admittances in parallel add,

\[
Y_L = \frac{1}{-jX_{C1}} + \frac{1}{R_s + jX_{C1}} = \frac{R_s + jX_{C1} - jX_{C1}}{(-jX_{C1})(R_s + jX_{C1})} = \frac{R_s}{X_{C1}^2 - jR_s X_{C1}}
\]

The reciprocal of the total load admittance produces the load impedance.
\[
Z_L = \frac{1}{Y_L} = \frac{X_{C1}^2 - jR_sX_{C1}}{R_s}
\]

\[Z_L = \frac{X_{C1}^2}{R_s} - jX_{C1}\]  
(15-45)

where \(Z_L\) is the ac load across the output of the amplifier used in the Pierce oscillator.

The gain (\(\beta'\)) from the amplifier's output to capacitor \(C_1\) is defined in Fig. 15-31(c). Thus

\[
\beta' = \frac{V_{out}}{V_{out}} = \frac{Z_L}{Z_{out} + Z_L}
\]  
(15-46)

where \(\beta'\) is the loaded gain from the amplifier's output to the input of a Pierce oscillator's feedback network. The gain from capacitor \(C_1\) to capacitor \(C_2\) is also defined in Fig. 15-31(c). Hence

\[
\beta'' = \frac{V_f}{V'_{out}} = \frac{-jX_{C2}}{R_s + jX_{C1}}
\]  
(15-47)

where \(\beta''\) is the gain of the feedback network used in the Pierce oscillator. The overall feedback factor can now be determined from

\[
\beta = \frac{V_f}{V_{out}} = \frac{V'_{out}}{V_{out}} \frac{V_f}{V'_{out}} = \beta'\beta''
\]  
(15-48)

where \(\beta\) is the overall feedback factor of the Pierce oscillator, which includes the loading on the amplifier's output.

---

**EXAMPLE 15-16**

Determine the ideal \(\beta\) and the actual \(\beta\) of the Pierce oscillator given in Fig. 15-30(a). Assume that the circuit oscillates at 999.850 kHz. The impedances have been given in Fig. 15-31(a).

**SOLUTION**

Ideally,

\[\beta = \frac{C_1}{C_2} = \frac{-250 \text{ pF}}{680 \text{ pF}} = -0.368\]

To determine the actual \(\beta\) we must first find the load across the amplifier's output. From Eq. 15-45,

\[
Z_L = \frac{X_{C1}^2}{R_s} - jX_{C1} = \frac{(636.7)^2}{125} - j636.7
\]

\[= 3243 - j636.7 \Omega = 3305 \Omega \angle -11.1^\circ\]
Now we can determine $\beta'$ by using Eq. 15-46.

$$\beta' = \frac{Z_c}{Z_L + Z_{out}} = \frac{3305 \angle -11.1^\circ}{(3243 - j636.7) + 20 \, k\Omega} = 0.142 \angle -9.5^\circ$$

$\beta''$ is given by using Eq. 15-47.

$$\beta'' = \frac{-jX_{C_2}}{R_s + jX_{C_1}} = \frac{-j234.1}{125 + j636.7} = 0.361 \angle -169^\circ$$

The actual $\beta$ is determined by Eq. 15-48.

$$\beta = \beta'\beta'' = (0.142 \angle -9.5^\circ)(0.361 \angle -169^\circ) = 0.0513 \angle -178.5^\circ = -0.0513$$

Obviously, there is a considerable discrepancy between the ideal and the actual feedback factor. The idealization is simply not a valid approximation. ■

Like all devices, crystals also have maximum ratings. For example, the dc voltage impressed across a crystal must be well below its maximum rating. If such a danger exists, a dc blocking capacitor should be placed in series with the crystal.

Even if the dc levels across the crystal are within acceptable limits, we must avoid overdriving it. Crystals have a maximum (ac) power rating. It is typically referred to as the crystal’s maximum drive level. The power dissipation within a crystal may be thought of as a power dissipation within the crystal’s equivalent series resistance ($R_s$).

Maximum drive levels range from as low as 0.1 mW to as high as 10 mW. The drive level rating is closely associated with the crystal’s geometry, or cut. The most common quartz crystal—the AT cut—is used in the frequency range 500 kHz to 100 MHz, and has a typical maximum drive level of 10 mW.

If a crystal used in an oscillator becomes overdriven, the frequency will be reduced or become unstable. (If the crystal is sufficiently overdriven, it may become fractured, and oscillations will cease.) Therefore, we must take steps to ensure that the crystal is not overdriven.

One technique to limit the drive level is to place an impedance (typically, a resistor) in series with the output of the amplifier. This has been illustrated in Fig. 15-32(a). A practical circuit has been given in Fig. 15-32(b).

The oscillator in Fig. 15-32(b) employs an M-tron MP-2 (AT-cut) crystal. The manufacturer states that its maximum series equivalent resistance is 500 $\Omega$, and its maximum drive level is 10 mW. The manufacturer also recommends drive levels on the order of 100 $\mu$W for maximum stability. Let us analyze Fig. 15-32(b).

The dc equivalent circuit of Fig. 15-32(b) has been indicated in Fig. 15-33(a). Diode $D_1$ has been added to provide a measure of temperature compensation for $Q_1$’s dc base bias. The 1N4148 small-signal silicon diode in the base circuit helps the collector current of the transistor remain constant with changes in temperature. (This technique was introduced in Section 12-14. However, in this case a single diode is being used.)

EXAMPLE

15-17

Perform a dc analysis of the Pierce oscillator given in Fig. 15-32(b). Determine the approximate values of $V_B$, $V_E$, and $I_C$. 884

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FIGURE 15-32 Improving the short-term stability of the Pierce oscillator: (a) using a resistor to restrict the crystal’s drive level; (b) practical circuit.

SOLUTION Using the dc equivalent circuit given in Fig. 15-33(a), we can see that

\[ V_B = V_{TH} = \frac{R_2}{R_1 + R_2} \left( V_{CC} - 0.7 \, \text{V} \right) + 0.7 \, \text{V} \]

\[ = \frac{4.7 \, \text{k\Omega}}{15 \, \text{k\Omega} + 4.7 \, \text{k\Omega}} \left( 9 \, \text{V} - 0.7 \, \text{V} \right) + 0.7 \, \text{V} = 2.68 \, \text{V} \]

\[ V_E = V_B - V_{BE} = 2.68 \, \text{V} - 0.7 \, \text{V} = 1.98 \, \text{V} \]

\[ I_C = I_E = \frac{V_E}{R_3} = \frac{1.98 \, \text{V}}{1 \, \text{k\Omega}} = 1.98 \, \text{mA} \]
FIGURE 15-33 Analyzing the improved circuit: (a) dc equivalent circuit; (b) design constraints on $C_1$ and $C_2$; (c) ac equivalent circuit; (d) the crystal’s in-circuit $Q$ will be large.

The ac equivalent circuit of Fig. 15-32(b) has been shown in Fig. 15-33(b). Our next step is to determine the BJT’s ac parameters.

**EXAMPLE 15-18**

Determine $g_m$, $r_o$, and $r_e$ for the 2N3904 BJT used in the Pierce oscillator given in Fig. 15-32(b).

**SOLUTION** First we shall determine the BJT’s $g_m$ at its quiescent collector current

$$g_m = \frac{I_c}{26 \text{ mV}} = \frac{1.98 \text{ mA}}{26 \text{ mV}} = 76.2 \text{ mS}$$

Now we find $r_o$.

$$r_o = \frac{200 \text{ V}}{I_c} = \frac{200 \text{ V}}{1.98 \text{ mA}} = 101 \text{ k}\Omega$$
The 2N3904 has an $h_{fe}$ of approximately 140 at an $I_C$ of 2 mA. Hence

$$r_n = \frac{h_{fe}}{g_m} = \frac{140}{76.2 \text{ mS}} = 1.84 \text{ k\Omega}$$

**EXAMPLE 15-19**

Determine $Z_{in}$, $Z_{out}$, $A_{v(oc)}$, and the (loaded) voltage gain $A_v$ for the amplifier used in the Pierce oscillator given in Fig. 15-32(b).

**SOLUTION** To determine $Z_{in}$, we ignore the diode’s dynamic resistance. It will be much, much smaller than $R_2$.

$$Z_{in} = R_1 \parallel R_2 \parallel r_n = 15 \text{ k\Omega} \parallel 4.7 \text{ k\Omega} \parallel 1.84 \text{ k\Omega} = 1.21 \text{ k\Omega}$$

No collector resistor is used and $L_1$ is an RFC with an $X_L$ of 628 k\Ω at $f_o$. Therefore, $Z_{out}$ is

$$Z_{out} = r_o = 101 \text{ k\Omega}$$

The open-circuit voltage gain is

$$A_{v(oc)} = -g_m r_o = -(76.2 \text{ mS})(101 \text{ k\Omega}) = -7696$$

To find $A_v$ we must first determine $r_C$.

$$r_C = r_o \parallel R_L = 101 \text{ k\Omega} \parallel 82 \text{ k\Omega} = 45.3 \text{ k\Omega}$$

and $A_v$ is

$$A_v = -g_m r_C = -(76.2 \text{ mS})(45.3 \text{ k\Omega}) = 3452$$

For good frequency stability, the crystal’s external load [$Z_{(XTAL \ load)}$ in Fig. 15-33(c)] should be as nonresistive as possible. If $X_{C1}$ and $X_{C2}$ are small, the resistive component of the load across the crystal will be negligibly small. As a rough rule of thumb, the reactances $X_{C1}$ and $X_{C2}$ are sized such that their magnitudes are on the same order as $R_s$. [The specifics are detailed in Fig. 15-33(d).] The symbol $X_{C(\text{XTAL \ load})}$ is the crystal’s equivalent load capacitance. The symbol $R_{(\text{XTAL \ load})}$ is the crystal’s equivalent load resistance. This will ensure that the crystal’s in-circuit $Q$ is large.

$$Q_{(\text{in-circuit})} = \frac{X_{L(\text{net})}}{R_s + R_{(\text{XTAL \ load})}}$$

The smaller this term is, the closer the $Q_{(\text{in-circuit})}$ will be to the $Q$ of the crystal.

**EXAMPLE 15-20**

Given the Pierce oscillator in Fig. 15-32(b), determine if the capacitor values are adequately large, and find the $Z_L$ across the amplifier’s output. The frequency of oscillation is 999.830 kHz.
SOLUTION First we determine \( X_{C1} \) and \( X_{C2} \).

\[
X_{C1} = \frac{1}{2\pi f_0 C_1} = \frac{1}{2\pi(999.830 \text{ kHz})(0.001 \mu\text{F})} = 159.2 \Omega
\]

\[
X_{C2} = \frac{1}{2\pi f_0 C_2} = \frac{1}{2\pi(999.830 \text{ kHz})(0.0015 \mu\text{F})} = 106.1 \Omega
\]

We observe that

\[
X_{C1} = 159.2 \Omega < Z_{\text{out}} + R = 103.7 \text{k}\Omega
\]

\[
X_{C2} = 106.1 \Omega < Z_{\text{in}} = 1.21 \text{k}\Omega
\]

The capacitive reactances seem reasonable since the MP-2 crystal has a typical \( R_s \) of 125 \( \Omega \) and an \( R_{\text{max}} \) of 500 \( \Omega \). Since the reactance levels are on the same order as the magnitude of \( R_s \), a high \( Q \) will result. However, we must use Eq. 15-45 to find the load across the amplifier's output.

\[
Z_L = \frac{X_{C1}^2}{R_s} = \frac{159.2^2 \Omega}{500 \Omega} = j159.2 \Omega
\]

\[
= 50.69 - j159.2 \Omega = 167.1 \Omega \angle -72.34^\circ
\]

EXAMPLE 15-21

Determine the loop gain of the Pierce oscillator given in Fig. 15-32(b).

SOLUTION First we find \( \beta' \). The total \( Z_{\text{out}} \) includes \( R_s \) and \( R_L \). Hence

\[
Z_{\text{out}} = R_s + R_L = 2.7 \text{k}\Omega + 101 \text{k}\Omega + 82 \text{k}\Omega = 48 \text{k}\Omega
\]

\[
\beta' = \frac{Z_L}{Z_{\text{out}} + Z_L} = \frac{167.1 \Omega \angle -72.34^\circ}{48 \text{k}\Omega + 50.69 \Omega - j159.2 \Omega}
\]

\[
= 3.478 \times 10^{-3} \angle -72.15^\circ
\]

Now we find \( \beta'' \).

\[
\beta'' = \frac{-jX_{C2}}{R_s + jX_{C1}} = \frac{-j106.1 \Omega}{500 \Omega + j159.2 \Omega} = \frac{106.1 \Omega \angle -90^\circ}{524.7 \Omega \angle 17.66^\circ}
\]

\[
= 0.2022 \angle -107.66^\circ
\]

The total feedback factor \( \beta \) is

\[
\beta = \beta' \beta'' = (3.478 \times 10^{-3} \angle -72.15^\circ)(0.2022 \angle -107.66^\circ)
\]

\[
= 0.000703 \angle -179.81^\circ = -0.000703
\]

Now we can find the loop gain.

\[
\beta A_v = (-0.000703)(-3452) = 2.43 > 1
\]

Therefore, the circuit is definitely going to oscillate.

The last step in our analysis of the Pierce oscillator is the determination of the crystal's drive level. When the oscillator is first powered up, we are dealing with small signals. As the oscillations grow in amplitude, we eventually enter the large-signal domain. The maximum possible output signal level has been illustrated in Fig. 15-34(a). The resulting large-signal equivalent circuit of the Pierce oscillator [Fig. 15-32(b)] has been given in Fig. 15-34(b).
EXAMPLE 15-22

Determine the maximum drive level the crystal will experience in Fig. 15-32(b).

SOLUTION As we can see in Fig. 15-34(b), the output voltage \( V_{\text{out}} \) is 4.95 V rms. By voltage division, we can ascertain \( V'_{\text{out}} \).

\[
V'_{\text{out}} = \frac{Z_L}{Z_L + R_d} V_{\text{out}} = \frac{167.1 \, \Omega \angle -72.3^\circ}{(50.7 \, \Omega - j159.2 \, \Omega) + 2.7 \, k\Omega}
\]

\[
= 300 \, \text{mV rms} \angle -69^\circ
\]

Now we can find the magnitude of the rms current through the crystal.

\[
I = \frac{V'_{\text{out}}}{R_{(\text{max})} + jX_{L(\text{net})}} = \frac{300 \, \text{mV rms} \angle -69^\circ}{500 \, \Omega + j265.3 \, \Omega}
\]

\[
|I| = 0.530 \, \text{mA rms} \angle -97^\circ
\]

The crystal's drive level can now be found.

\[
P_{\text{XTAL}} = |I|^2 R_{(\text{max})} = (0.530 \, \text{mA rms})^2 (500 \, \Omega)
\]

\[
= 140 \, \mu\text{W}
\]
FIGURE 15-35 Crystal-controlled Colpitts oscillator: (a) circuit; (b) dc equivalent; (c) the ac equivalent reveals that we have a common-base BJT amplifier.

The 140 \( \mu \)W of power dissipation is much less than the crystal's maximum rating of 10 mW, and on the order of the manufacturer's recommended nominal drive level of 100 \( \mu \)W. As we can see in Fig. 15-32(b), the actual \( V_{\text{out}} \) was only 4 V peak to peak. Running through the same calculations, we see that the crystal's drive level is only 13.3 \( \mu \)W.

A rough check of the drive level of a crystal in an oscillator can be made by varying \( V_{\text{CC}} \). Normally, increasing \( V_{\text{CC}} \) will produce a slight increase in the oscillator's output frequency. If the crystal is being overdriven, increasing \( V_{\text{CC}} \) will result in a decrease in the output frequency, or the output frequency will become unstable.

Using this check, the Pierce oscillator in Fig. 15-32(b) performed very well. \( V_{\text{CC}} \) was adjusted from 6 to 20 V and its output frequency remained "solid" at 999.830 kHz.

The last crystal oscillator we shall investigate is shown in Fig. 15-35. The circuit may be described as a crystal-controlled Colpitts oscillator. The basic configuration has performed well in applications ranging from 1 MHz to over 30 MHz.

Considerable attention has been paid to decoupling. Three RFCs are used [see \( L_2, L_3, \) and \( L_4 \) in Fig. 15-35(a)]. Capacitors \( C_3 \) and \( C_4 \) provide additional decoupling. The dc equivalent circuit has been shown in Fig. 15-35(b).
The ac equivalent circuit has been given in Fig. 15-35(c). The BJT is in its common-base configuration. (The output is at the collector, and the input is at the emitter.) The crystal is operated in its series resonant mode to place the base of the BJT at ac ground. The inductor $L_1$ is slug tuned. This allows the output frequency to be adjusted over a narrow range.

15-16 UJT Relaxation Oscillators

In Section 15-1 we mentioned that the two basic oscillator categories are harmonic and relaxation. The block diagram of the relaxation oscillator is given in Fig. 15-36.

The circuit oscillates as energy is exchanged between the time constant network and the active device. The output waveforms produced by relaxation oscillators are invariably nonsinusoidal. Typical examples (the "sawtooth," triangular, and rectangular waveforms) have been indicated in Fig. 15-36.

A relatively simple relaxation oscillator can be constructed around a device called the unijunction transistor (UJT). In its simplest form, the UJT is made by diffusing a $p$-type region into a lightly doped $n$-type ($n^-$) silicon crystal [see Fig. 15-37(a)]. The resulting $p$-$n$ junction is located about 70% of the crystal's length away from the base 1 end of the structure. The three terminals of the UJT are the base 1 ($B_1$), base 2 ($B_2$), and the emitter ($E$).

UJTs are packaged in much the same manner as small-signal BJTs. For example, the 2N2646 and 2N2647 UJTs are available in the modified TO-18 case style shown in Fig. 15-37(b). The UJT's schematic symbol is given in Fig. 15-37(c).

The electrically equivalent circuit of a UJT is shown in Fig. 15-38(a). The diode is used to represent the $p$-$n$ junction between the $p$ region and the $n^-$ region. The resistors $R_{B1}$ and $R_{B2}$ are used to represent the resistance of the lightly doped ($n^-$) semiconductor.

The resistance between the $B_1$ and $B_2$ terminals is called the interbase resistance. Its symbol is $R_{BB}$. Typical values range from 4 to 10 kΩ. The interbase resistance is measured with the emitter open [see the test circuit shown in Fig. 15-38(b)].

$$R_{BB} = R_{B1} + R_{B2} \bigg|_{I_E=0}$$  \hspace{1cm} (15-49)

where $R_{BB}$ is the interbase resistance parameter of the UJT.

**FIGURE 15-36** Block diagram of a relaxation oscillator.
As can be seen in Fig. 15-38(a), base 2 is connected to a positive source \( V_{BB} \) and base 1 is returned to ground. As a result of the (conventional) current flow from base 2 to base 1, there is a voltage gradient along the length of the \( n^- \) silicon structure. Therefore, we have a voltage in the region of the emitter junction which is positive with respect to ground.

The magnitude of this voltage is given by the simple voltage-divider action between \( R_{B1} \) and \( R_{B2} \).

\[
V = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{B2B1} = \eta V_{BB}
\]

(15-50)

The Greek letter \( \eta \) (eta) is called the intrinsic stand-off ratio. This parameter is also available on most UJT data sheets.

The voltage \( V \) defined in Eq. 15-50 is the positive potential that appears on the \( n^- \)-side of the emitter's \( p-n \) junction. The emitter junction is reverse biased until the voltage between the emitter terminal and base 1 becomes more positive than the voltage \( V \). Allowing 0.5 V (at 25°C) to be the voltage drop across the \( p-n \) junction, the required emitter-base 1 voltage to just cause emitter conduction is

\[
V_p = 0.5 \text{ V} + \eta V_{B2B1}
\]

(15-51)

The symbol \( V_p \) is used to represent the UJT's peak-point voltage.

When \( V_{B2B1} \) is equal to \( V_p \), the emitter junction becomes forward biased and holes from the emitter are injected into the \( n^- \) silicon structure. These holes travel from the emitter toward the base 1 region. The holes in the base 1 region attract electrons from ground.

Since the conductivity of any semiconductor material is a direct function of the number of electrons per unit of volume, the resistance between the emitter and ground
is greatly reduced. As a result, emitter current rises while the voltage between the emitter and base 1 terminal decreases. This gives the emitter–base 1 region a negative resistance characteristic.

After a certain point, any further increases in the emitter current will start to increase the voltage drop between the emitter and base 1. This is referred to as the UJT's saturation region. This will occur when the rate of hole injection is so great as to build up a "positive space charge" in the base 1 region.

The UJT's resulting emitter (or input) V-I characteristic curve has been given in Fig. 15-38(c). To emphasize the UJT's peak and valley, it is customary to interchange the voltage and current axes as indicated in the figure. By inspection of Fig. 15-38(c) we can see that $I_p$, the peak-point current, represents the minimum amount of emitter current to place the UJT in its negative resistance region. The valley current $I_v$ is the maximum emitter current within the negative resistance region. Similarly, the valley voltage $V_v$ is the minimum voltage that can maintain the UJT in its negative resistance region. The peak-point voltage $V_p$ was defined in Eq. 15-51.
The actual emitter characteristic of a 2N2646 UJT was developed in the laboratory. The resulting V-I curve has been indicated in Fig. 15-38(d). The indicated values agree with the values found on the manufacturer's data sheet.

For a UJT to function properly in an oscillator, its dc load line must cross the negative resistance region of its emitter characteristic. This has been detailed in Fig. 15-39. Figure 15-39(a) shows the dc equivalent circuit. The dc load line has been constructed in Fig. 15-39(b).

By inspection of Fig. 15-39(c), we can determine the minimum and maximum values of \( R_E \) required. Thus

\[
R_{E(\max)} = -\frac{\Delta V}{\Delta I} = -\frac{V_{BB} - V_P}{0 - I_P} = \frac{V_{BB} - V_P}{I_P}
\]

and

\[
R_{E(\min)} = -\frac{\Delta V}{\Delta I} = -\frac{V_{BB} - V_V}{0 - I_V} = \frac{V_{BB} - V_V}{I_V}
\]

(Fig. 15-39) UJT's dc load line: (a) dc circuit; (b) dc load line; (c) minimum and maximum values of \( R_E \) required for oscillation.
The design rule for $R_E$ is given by

$$\frac{V_{BB} - V_V}{I_V} \leq R_E \leq \frac{V_{BB} - V_P}{I_P} \quad (15-52)$$

where $R_E$ is the emitter resistance required to ensure UJT circuit oscillation.

A basic UJT relaxation oscillator circuit has been given in Fig. 15-40(a). Its operation is relatively simple. When power is first applied, capacitor $C_1$ will begin to charge through resistor $R_E$. (The emitter–base 1 diode will be reverse biased. Therefore, the emitter current will be approximately zero.) The voltage across the capacitor will attempt to reach $V_{BB}$. However, when the voltage across the capacitor

**FIGURE 15-40** UJT relaxation oscillator: (a) practical UJT relaxation oscillator; (b) actual waveforms; (c) analyzing the capacitor's charge time ($t_1$) to find the approximate period ($T$).
reaches $V_P$, the resistance between the emitter and base 1 decreases. Simply, the UJT’s emitter goes into conduction, or “fires.” The sudden increase in the emitter current will serve to discharge the capacitor quickly.

During conduction, the capacitor serves as the driving potential. The capacitor’s discharge current is limited by the base 1 resistor $R_1$, and the dynamic resistance of the emitter diode. When the capacitor discharges to the point where the voltage across it is approximately equal to $V_V$, the emitter diode stops conducting, and becomes open again. At this point the capacitor will again start to charge toward $V_{BB}$, and the cycle is repeated.

The charge and discharge of capacitor $C_1$ produces a sawtooth type of waveform. Voltage “spikes” will be produced at the UJT’s base 1 and base 2 terminals. Actual waveforms are indicated in Fig. 15-40(b).

As can be seen in Fig. 15-40(b), the period of the voltage waveform across $C_1$ is approximately equal to the capacitor’s charge time. The equation describing this charging action is

$$v_c = V_f + (V_F - V_f)(1 - e^{-tv})$$

(15-53)

where $v_c$ = instantaneous capacitor voltage
$V_f$ = initial capacitor voltage
$V_F$ = final voltage to which the capacitor attempts to charge
$e$ = natural number 2.718 $\cdots$
$\tau$ = (tau) the $RC$ time constant

For our problem we are interested in finding the length of time required for the capacitor to charge from $V_V$ to $V_P$. The capacitor is attempting to charge to $V_{BB}$ [see Fig. 15-40(c)]. Hence, from Eq. 15-53,

$$V_P = V_V + (V_{BB} - V_V)(1 - e^{-tv})$$

(15-54)

We must solve this relationship for $t_V$ since it is approximately equal to the period ($T$) of the output waveform. This will give us an equation for the frequency of oscillation.

$$(1 - e^{-tv}) = \frac{V_P - V_V}{V_{BB} - V_V}$$

In a “real” UJT circuit,

$V_P > V_V$ and $V_{BB} >> V_V$

$$1 - e^{-tv} = \frac{V_P - V_V}{V_{BB} - V_V} = \frac{V_P}{V_{BB}}$$

To simplify our work further, we can state that

$$V_P = 0.5 V + \eta V_{BB1} = \eta V_{BB1} = \eta V_{BB}$$

The resistors in series with the base 1 and base 2 terminals are very small [refer to Fig. 15-40(a)]. Consequently, $V_{BB1}$ is approximately equal to $V_{BB}$. Thus

$$1 - e^{-tv} = \frac{V_P}{V_{BB}} = \frac{\eta V_{BB}}{V_{BB}} = \eta$$

$$-e^{-tv} = \eta - 1$$

Multiplying both sides by $-1$ gives us

$$e^{-tv} = 1 - \eta$$
Inverting both sides gives us

\[ e^{\frac{1}{1-\eta}} = \frac{1}{1-\eta} \]

To solve for \( t_1 \) we must take the natural logarithm of both sides.

\[ t_1 = \ln \frac{1}{1-\eta} \]

\[ t_1 = T = \tau \ln \frac{1}{1-\eta} \]

The time constant \( \tau \) is given by

\[ \tau = R_E C_1 \]

and

\[ T = R_E C_1 \ln \frac{1}{1-\eta} \]

\[ \frac{1}{T} = \frac{1}{R_E C_1 \ln \left( \frac{1}{1-\eta} \right)} \]

(15-54)

where \( f_o \) is the UJT relaxation oscillator's oscillation frequency.

**EXAMPLE 15-23**

Analyze the UJT relaxation oscillator given in Fig. 15-40(a). Specifically, verify that \( R_E \) is properly sized, and determine \( f_o \).

**SOLUTION** To check the value of \( R_E \), we must have UJT data. The indicated 2N2646 has the following parameters:

\[ V_p = 7.8 \text{ V} \quad V_V = 2 \text{ V} \]
\[ I_p = 1 \mu\text{A} \quad I_V = 2 \text{ mA} \]

From Eq. 15-52,

\[ \frac{V_{BB} - V_V}{I_V} \leq R_E \leq \frac{V_{BB} - V_p}{I_p} \]
\[ \frac{12 \text{ V} - 2 \text{ V}}{2 \text{ mA}} \leq R_E \leq \frac{12 \text{ V} - 7.8 \text{ V}}{2 \mu\text{A}} \]
\[ 5 \text{ k}\Omega \leq R_E \leq 4.2 \text{ M}\Omega \]

Therefore, an \( R_E \) of 10 k\( \Omega \) appears to be a reasonable value. The circuit will oscillate. The \( \eta \) of the 2N2646 is 0.6. Now we may use Eq. 15-54 to find \( f_o \).

\[ f_o = \frac{1}{R_E C_1 \ln \left( \frac{1}{1-\eta} \right)} \]

\[ = \frac{1}{(10 \text{ k}\Omega)(0.1 \mu\text{F}) \ln \left( \frac{1}{1-0.6} \right)} \]

\[ = 1091 \text{ Hz} \]
The actual measured waveforms have been given in Fig. 15-40(b). Their frequency was 863 Hz. This is about 21% lower than our calculated value. Considering our approximations and the tolerances of \( R_E \) and \( C_1 \), this is a reasonable result. If the frequency is to be trimmed, "\( R_E \)" should be a fixed resistor (e.g., 9.1 kΩ) in series with a potentiometer (e.g., a 2-kΩ unit).

### 15-17 An Op Amp Relaxation Oscillator

The op amp relaxation oscillator shown in Fig. 15-41(a) is a square-wave generator. In general, square waves are relatively easy to produce. Like the UJT relaxation oscillator, the circuit's frequency of oscillation is dependent on the charge and discharge of a capacitor (\( C_1 \)) through a resistor (\( R_I \)). The "heart" of the oscillator is an inverting op amp comparator (refer to Fig. 15-41(b)). The comparator uses positive feedback.

Positive feedback increases the gain of an amplifier. In a comparator circuit this offers two advantages. First, the high gain causes the op amp's output to switch

**FIGURE 15-41 Op amp relaxation oscillator: (a) circuit; (b) the "heart" of the oscillator is an inverting op amp comparator.**
very quickly from rail to rail. Second, the use of positive feedback gives the circuit hysteresis. Since the comparator is fundamental to the operation of the square-wave generator, and an important circuit in its own right, it deserves our serious attention. The operation of the inverting comparator has been detailed in Fig. 15-42.

The comparator is a nonlinear circuit. Its output assumes one of two states. It is either at the positive supply rail (+$V_{\text{sat}}$) or at the negative supply rail ($-V_{\text{sat}}$).

**FIGURE 15-42** Operation of the inverting comparator and its composite transfer characteristic curve (a).

To get the comparator's output to switch, $V_{\text{IN}}$ must be more positive than $\beta V_{\text{sat}}$

\[
V_{\text{IN}} = \frac{R_4}{R_3 + R_4} V_{\text{sat}} = \beta V_{\text{sat}}
\]

(a)

Once the comparator's output has switched to $-V_{\text{sat}}$, $V_{\text{IN}}$ must be more negative than $-\beta V_{\text{sat}}$ to make the output go to $+V_{\text{sat}}$

\[
V_{\text{F}} = -\beta V_{\text{sat}}
\]

(c)

\[
V_{\text{OUT}} = -V_{\text{sat}} = \beta V_{\text{sat}}
\]

(d)

\[
V_{\text{OUT}} = 0
\]

(e)

Hysteresis = $V_{\text{UTP}} - V_{\text{LTP}} = 2\beta V_{\text{sat}}$
In Fig. 15-42(a) we have assumed that the output is at \( +V_{\text{SAT}} \). Since the op amp’s noninverting input terminal draws negligible current, we may find the feedback voltage \( v_F \) by simple voltage division.

\[
v_F = \frac{R_4}{R_3 + R_4} \cdot \text{vout} = \frac{R_4}{R_3 + R_4} \cdot (+V_{\text{SAT}})
\]

Let

\[
\beta = \frac{R_4}{R_3 + R_4}
\]

and we arrive at

\[
v_F = \beta (+V_{\text{SAT}}) \quad (15-55)
\]

As we can see in Fig. 15-42(a), to get the op amp to switch from \( +V_{\text{SAT}} \) to \( -V_{\text{SAT}} \), \( v_{\text{IN}} \) must be slightly more positive than \( v_F \). This particular value of \( v_{\text{IN}} \) is called the comparator’s upper trigger point \( V_{\text{UTP}} \). A graph of the input-output relationship is given in Fig. 15-42(b).

Once the output of the op amp has switched to \( -V_{\text{SAT}} \), a negative (feedback) voltage appears at the op amp’s noninverting input terminal. Hence

\[
v_F = \beta (-V_{\text{SAT}}) \quad (15-56)
\]

Figure 15-42(c) illustrates that \( v_{\text{IN}} \) must now be more negative than \( v_F \) to get the op amp’s output to switch back to \( +V_{\text{SAT}} \). This particular value of \( v_{\text{IN}} \) is called the comparator’s lower trigger point \( V_{\text{LTP}} \). A graph of this input-output relationship is provided in Fig. 15-42(d).

The composite transfer characteristic curve is shown in Fig. 15-42(e). If the output is positive, \( v_{\text{IN}} \) must be increased to a value slightly greater than the upper trigger point \( V_{\text{UTP}} \). When this occurs the output will switch to \( -V_{\text{SAT}} \). To get the output to switch back to \( +V_{\text{SAT}} \), \( v_{\text{IN}} \) must be made slightly more negative than the lower trigger point \( V_{\text{LTP}} \).

The difference between \( V_{\text{UTP}} \) and \( V_{\text{LTP}} \) is called the comparator’s hysteresis \( H \) [see Fig. 15-42(e) and Eq. 15-57].

\[
\boxed{H = V_{\text{UTP}} - V_{\text{LTP}}} \quad (15-57)
\]

where \( H \) = hysteresis

\[
V_{\text{UTP}} = \text{upper trigger point} = \beta (+V_{\text{Sat}})
\]
\[
V_{\text{LTP}} = \text{lower trigger point} = \beta (-V_{\text{Sat}})
\]

An op amp’s output saturation voltages \((+V_{\text{SAT}} \text{ and } -V_{\text{SAT}})\) are not well defined.

We can more precisely determine the output voltage by using back-to-back zener diodes [see Fig. 15-41(a)]. When the op amp’s output switches to \( +V_{\text{SAT}} \), zener diode \( D_1 \) enters breakdown and zener diode \( D_2 \) becomes forward biased. Similarly, when the op amp’s output switches to \( -V_{\text{SAT}} \), zener diode \( D_2 \) enters breakdown and zener diode \( D_1 \) becomes forward biased. Therefore, the output voltage becomes

\[
v_{\text{OUT}} = \pm (V_z + 0.7 \text{ V})
\]

and

\[
v_F = \beta (V_z + 0.7 \text{ V})
\]
Therefore, not only does the output voltage become more well defined, but so do the comparator's upper and lower trigger points.

Resistor $R_2$ is included to limit the op amp's output current. Since most op amps include output short-circuit protection, its use is optional and falls in the 'good practice' category. Now that we understand the operation of the inverting comparator, let us consider the operation of the square-wave generator [Fig. 15-41(a)].

When the output of the comparator is positive, capacitor $C_1$ will charge through resistor $R_1$. The capacitor will attempt to charge to $v_{\text{OUT}}$.

$$v_{\text{OUT}} = V_Z + 0.7 \text{ V}$$

When the voltage across the capacitor reaches the upper trigger point,

$$V_{\text{UTP}} = v_F = \beta v_{\text{OUT}} = \beta(V_Z + 0.7 \text{ V})$$

and the comparator's output will immediately switch negative.

$$v_{\text{OUT}} = -(V_Z + 0.7 \text{ V})$$

The capacitor will then start to charge from the positive upper trigger point voltage toward the negative output voltage.

When the voltage across the capacitor reaches the lower trigger point,

$$V_{\text{LTP}} = v_F = \beta v_{\text{OUT}} = -\beta(V_Z + 0.7 \text{ V})$$

the output will again go positive, and the cycle repeats. The waveforms associated with the circuit have been given in Fig. 15-41(a).

To derive an equation for the output frequency, we shall draw on Eq. 15-53. With reference to Fig. 15-41(a), the substitutions below to find the charge time $t_i$ become clear.

$$v_c = V_i + (V_F - V_i)(1 - e^{-ni\tau})$$

$$\beta v_{\text{OUT}} = -\beta v_{\text{OUT}} + [v_{\text{OUT}} - (-\beta v_{\text{OUT}})](1 - e^{-ni\tau})$$

$$= -\beta v_{\text{OUT}} + (v_{\text{OUT}} + \beta v_{\text{OUT}})(1 - e^{-ni\tau})$$

Dividing both sides by $v_{\text{OUT}}$, we have

$$\beta = -\beta + (1 + \beta)(1 - e^{-ni\tau})$$

$$2\beta = (1 + \beta)(1 - e^{-ni\tau})$$

Continuing, we have

$$1 - e^{-ni\tau} = \frac{2\beta}{1 + \beta}$$

$$-e^{-ni\tau} = \frac{2\beta}{1 + \beta} - 1 = \frac{2\beta - (1 + \beta)}{1 + \beta} = \frac{\beta - 1}{1 + \beta}$$

Multiplying both sides by $-1$ yields

$$e^{-ni\tau} = \frac{1 - \beta}{1 + \beta}$$

Inverting both sides gives us

$$e^{ni\tau} = \frac{1 + \beta}{1 - \beta}$$

We may solve for $t_i$ by taking the natural log of both sides.

$$\frac{t_i}{\tau} = \ln \frac{1 + \beta}{1 - \beta}$$
\[ t_1 = \tau \ln \frac{1 + \beta}{1 - \beta} = R_1 C_1 \ln \frac{1 + \beta}{1 - \beta} \]

By inspection of Fig. 15-41(a), we can see that the charge time \( t_1 \) from the lower trigger point to the upper trigger point is equal to the charge time from the upper trigger point to the lower trigger point. Alternatively, we can state that \( t_1 \) is equal to one-half of the period. Hence

\[ T = 2t_1 = 2R_1 C_1 \ln \frac{1 + \beta}{1 - \beta} \]

\[ f_o = \frac{1}{T} = \frac{1}{2R_1 C_1 \ln \left(\frac{1 + \beta}{1 - \beta}\right)} \quad (15-58) \]

where \( f_o \) is the output frequency of the op amp square-wave generator.

Recall that \( \beta \) is determined by simple voltage division between \( R_3 \) and \( R_4 \). We can simplify Eq. 15-58 if we implement the following constraint:

\[ R_4 = 0.859R_3 \]

Under this condition \( \beta \) is equal to 0.462, and

\[ \ln \frac{1 + \beta}{1 - \beta} = 1 \]

Therefore, Eq. 15-58 simplifies to

\[ f_o = \frac{1}{2R_1 C_1} \bigg|_{R_4=0.859R_3} \quad (15-59) \]

where \( f_o \) is the output frequency of the op amp square-wave generator.

**EXAMPLE 15-24**

Analyze the op amp square-wave generator given in Fig. 15-41(a). Determine the square-wave peak-to-peak output voltage. Is \( R_2 \) adequately sized? (Assume that \( +V_{SAT} \) is 13 V and \( I_{SC} \) is 10 mA.) Do \( R_3 \) and \( R_4 \) have the proper relationship? If so, use Eq. 15-59 to determine \( f_o \). Finally, determine the peak-to-peak value of the voltage across capacitor \( C_1 \).

**SOLUTION** Since the 1N757 is a 9.1-V zener diode, the positive peak output voltage will be 9.8 V. Similarly, the negative peak output voltage will be \(-9.8 \) V, and the resulting peak-to-peak output voltage will be 19.6 V. Specifically,

\[ v_{OUT(peak-to-peak)} = 2(V_Z + 0.7 \text{ V}) = 2(9.8 \text{ V}) = 19.6 \text{ V} \]

Now we shall investigate \( R_2 \). If \( +V_{SAT} \) is 13 V, the op amp’s output current \( I \) will be

\[ I = \frac{+V_{SAT} - (V_Z + 0.7 \text{ V})}{R_2} = \frac{13 \text{ V} - 9.8 \text{ V}}{330 \Omega} \]

\[ = 9.70 \text{ mA} < I_{SC} = 10 \text{ mA} \]
Therefore, $R_2$ appears to be adequately sized. Now we shall determine if $R_3$ and $R_4$ have the proper relationship to draw on Eq. 15-59.

\[
\frac{R_4}{R_3} = 0.859
\]

\[
\frac{R_4}{R_3} = \frac{8.6 \text{ k}\Omega}{10 \text{ k}\Omega} = 0.86 = 0.859
\]

Since the constraint on $R_3$ and $R_4$ appears to be satisfied, we may use Eq. 15-59 to determine $f_o$.

\[
f_o = \frac{1}{2RC_1} = \frac{1}{2(10 \text{ k}\Omega)(0.1 \mu\text{F})} = 1 \text{ kHz}
\]

To determine the peak-to-peak voltage across capacitor $C_1$, we first recognize that it will be equal to the comparator’s hysteresis.

\[
\beta = \frac{R_4}{R_3 + R_4} = \frac{8.6 \text{ k}\Omega}{10 \text{ k}\Omega + 8.6 \text{ k}\Omega} = 0.4624
\]

\[
v_F = \pm \beta v_{OUT} = \pm \beta (V_Z + 0.7 \text{ V})
\]

\[
= \pm (0.4624)(9.8 \text{ V}) = \pm 4.53 \text{ V} \rightarrow 9.06 \text{ V p-p}
\]

We conclude our discussion of the op amp square-wave generator by offering some additional “real-world” considerations. The circuit works reasonably well over the audio-frequency range. To decrease its frequency of oscillation, $C_1$ and/or $R_1$ must be increased. However, $C_1$ cannot be an electrolytic unit. This is true because electrolytics are polarized, and the capacitor must charge to a positive voltage ($V_{UTP}$) and to a negative voltage ($V_{UTN}$). Increasing $R_1$ to lower $f_o$ also reduces the available current to charge $C_1$. If $R_1$ is too large, the op amp’s input bias current will become significant. This can result in a radical departure from our theoretical calculations.

The maximum oscillation frequencies are limited by the op amp’s slew rate. Additional time delays occur as the op amp pulls out of saturation. Both the low-and the high-frequency restrictions can be circumvented by using a reasonably good op amp. Do not expect superior performance from the 741C op amp.

### 15-18 An Op Amp Triangle Generator

The op amp triangle generator is another example of a relaxation oscillator. The oscillator incorporates two stages: a noninverting comparator with hysteresis and an inverting integrator. As we can see in Fig. 15-43(a), the circuit simultaneously provides two different output waveforms. The comparator's output is a square wave, while the output of the integrator is a triangle wave.

We shall begin our analysis by first examining the noninverting comparator [see Fig. 15-43(b)]. The circuit is nonlinear and incorporates positive feedback. When $v_{IN}$ is positive enough, the noninverting input will be at a positive value. This will send the op amp's output to the positive supply rail (+ $V_{SAT}$). The output will remain at + $V_{SAT}$ even when $v_{IN}$ falls, and then goes negative. This is true because of the
voltage-divider action between $R_1$ and $R_2$. The large positive output voltage of $+V_{\text{SAT}}$ will continue to hold the noninverting input terminal positive even for small negative values of $v_{\text{IN}}$.

When $v_{\text{IN}}$ goes negative enough, the noninverting input terminal will become negative and send the output to the negative rail ($-V_{\text{SAT}}$). The output will remain at $-V_{\text{SAT}}$ even for small positive values of $v_{\text{IN}}$. Once again, the voltage divider action offered by $R_1$ and $R_2$ tends to hold the noninverting input terminal negative.

Since the circuit is nonlinear, the superposition theorem should not be used. However, we can apply Ohm's law and Kirchhoff's voltage law to analyze the circuit. The equivalent circuit is shown in Fig. 15-43(b). We have assumed that the op amp's noninverting input terminal draws a negligibly small input current.

First, we shall find $I$.

$$I = \frac{+V_{\text{SAT}} - V_{\text{IN}}}{R_1 + R_2}$$

**FIGURE 15-43** Op amp triangle wave generator and its noninverting comparator: (a) basic triangle-wave generator; (b) analyzing its noninverting comparator; (c) the output will be at $+V_{\text{SAT}}$ as long as $V_{\text{IN}}$ is more positive than $-(R_1/R_2)(+V_{\text{SAT}})$; (d) the output will be at $-V_{\text{SAT}}$ as long as $V_{\text{IN}}$ is more negative than $-(R_1/R_2)(+V_{\text{SAT}})$; (e) composite transfer characteristic curve.
FIGURE 15-43  (continued)

Now we shall find $V_A$ (the voltage at the noninverting input) by using Kirchhoff's voltage law.

$$V_A = +V_{SAT} - IR_2$$

By substitution we obtain

$$V_A = +V_{SAT} - \frac{(+V_{SAT} - V_{IN})R_2}{R_1 + R_2}$$

The comparator's output will switch from high ($+V_{SAT}$) to low ($-V_{SAT}$) when $V_A$ becomes slightly less than zero. Expanding and setting $V_A < 0$, we can solve for the required value of $V_{IN}$. 

An Op Amp Triangle Generator 905
\[ +V_{\text{SAT}} - \frac{R_2}{R_1 + R_2} (+V_{\text{SAT}}) + \frac{R_2}{R_1 + R_2} V_{\text{IN}} = V_A < 0 \]

\[ \frac{R_2}{R_1 + R_2} V_{\text{IN}} < \frac{R_2}{R_1 + R_2} (+V_{\text{SAT}}) - (+V_{\text{SAT}}) \]

\[ V_{\text{IN}} < +V_{\text{SAT}} - \frac{R_1 + R_2}{R_2} (+V_{\text{SAT}}) \]

\[ V_{\text{IN}} < \frac{R_2 - R_1 - R_2}{R_2} (+V_{\text{SAT}}) = -\frac{R_1}{R_2} (+V_{\text{SAT}}) \]

The result above tells us how negative \( V_{\text{IN}} \) must be to get the output to switch from \( +V_{\text{SAT}} \) to \( -V_{\text{SAT}} \). This is the comparator's lower trigger point [see Fig. 15-43(c)]. By symmetry, we can find the upper trigger point,

\[ V_{\text{IN}} > -\frac{R_1}{R_2} (-V_{\text{SAT}}) \]

to get the input voltage \( V_{\text{IN}} \) positive enough to cause the output to switch from \( -V_{\text{SAT}} \) to \( +V_{\text{SAT}} \) [see Fig. 15-43(d)]. The transfer characteristic curve summarizes the operation of the noninverting comparator [see Fig. 15-43(e)].

Since the comparator’s trigger points are determined by the op amp’s \( +V_{\text{SAT}} \) and \( -V_{\text{SAT}} \) output, some degree of precision is lost. However, by once again using zener diodes, it becomes possible to define the trip points more precisely. The use of output limiting, and the resulting transfer characteristic curve, is shown in Fig. 15-44.

**FIGURE 15-44 Improving the comparator's performance.**

(a)

(b)

\[ V_{LTP} = -\frac{R_1}{R_2} (V_Z + 0.7 \text{ V}) \]

\[ V_{UPT} = \frac{R_1}{R_2} (V_Z + 0.7 \text{ V}) = 1.20 \text{ V} \]

\[ -(V_Z + 0.7 \text{ V}) = -9.8 \text{ V} \]
EXAMPLE 15-25

Sketch the transfer characteristic curve of the noninverting comparator given in Fig. 15-44(a). Also determine the hysteresis.

**SOLUTION** The general shape of the curve has been given in Fig. 15-44(b). Therefore, our task is to determine the peak output voltages and the upper and lower trigger points. Since the output is clipped by a pair of back-to-back 9.1-V zeners, we recall from Example 15-24 that the output is ±9.8 V. If \( v_{\text{OUT}} = -9.8 \text{ V} \), \( v_{\text{IN}} \) must become positive enough to cause the output to switch. Hence

\[
v_{\text{IN}} = V_{\text{UTP}} = \frac{R_1}{R_2} (V_z + 0.7 \text{ V}) = \frac{100 \text{ k}\Omega}{820 \text{ k}\Omega} (9.8 \text{ V}) = 1.20 \text{ V}
\]

In a similar fashion, the positive output voltage will be 9.8 V, and the lower trigger point is

\[
v_{\text{IN}} = V_{\text{LTP}} = -\frac{R_1}{R_2} (V_z + 0.7 \text{ V}) = -\frac{100 \text{ k}\Omega}{820 \text{ k}\Omega} (9.8 \text{ V}) = -1.20 \text{ V}
\]

The hysteresis is the difference between the upper and lower trigger points.

\[
H = V_{\text{UTP}} - V_{\text{LTP}} = 1.20 \text{ V} - (-1.20 \text{ V}) = 2.40 \text{ V}
\]

Now let us consider the inverting integrator. It has been redrawn in Fig. 15-45(a). Notice that the input voltage has been shown to be a (constant) dc level \( V_{\text{IN}} \). The right end of resistor \( R_3 \) is at virtual ground. Therefore, all of \( V_{\text{IN}} \) is dropped across \( R_3 \). The resulting current is

\[
I = \frac{V_{\text{IN}}}{R_3}
\]

Since \( V_{\text{IN}} \) and \( R_3 \) are constants, it follows that \( I \) will also be constant.

Recall that the op amp’s output terminals draw negligible current. Therefore, all of the current \( I \) flows into the feedback loop. Consequently, the capacitor \( (C_1) \) is being charged by a constant current. To find the voltage developed across the capacitor, we must remind ourselves of two fundamental relationships. First,

\[
I = \frac{Q}{t}
\]

Therefore,

\[
Q = It
\]

Let us consider the meaning of this relationship. If the current \( I \) is a constant, the total charge is going to increase linearly with time. The second equation we must draw on describes the charge-voltage relationship of a capacitor. Specifically,

\[
Q = C_1v_{C_1}
\]

Solving for \( v_{C_1} \) gives us

\[
v_{C_1} = \frac{Q}{C_1}
\]

By substitution,

\[
v_{C_1} = \frac{Q}{C_1} = \frac{I}{C_1} t
\]
and for our op amp integrator,
\[ v_{C1} = \frac{I}{C_1} t = \frac{V_{IN}/R_3}{C_1} t = \frac{V_{IN}}{R_3 C_1} t \]

Turning again to Fig. 15-45(a), we see that the integrator's output voltage is equal to \(-v_{C1}\). This leads us to

\[ v_{OUT} = -v_{C1} = -\frac{V_{IN}}{R_3 C_1} t \]  \hspace{1cm} (15-60)

where \(v_{OUT}\) is the integrator's output voltage for a constant input voltage \(V_{IN}\).

Since \(V_{IN}\), \(R_3\), and \(C_1\) are constants, the output voltage will decrease linearly with time. If \(V_{IN}\) is a negative input voltage, the output voltage will increase linearly with time. Graphs of the integrator's output voltage for positive and negative input voltages have been given in Fig. 15-45(b) and (c), respectively.
The fact that a constant input voltage produces a linear ramp in the output voltage of an integrator is fundamental to the operation of the triangle generator. However, the op amp integrator is capable of providing an output voltage that is equal to the mathematical integral of the input voltage. This makes the op amp integrator an extremely useful "building block" in many electronic systems. The argument above used to explain the generation of a voltage ramp is actually a special case.

In calculus it is learned that mathematical integration allows us to find the area under a curve. If the input voltage is a constant, the area under it increases linearly with time. Therefore, a graph of the integral of a constant is a ramp. Just to familiarize the student with the mathematical notation used to describe the op amp inverting integrator, we present

\[
    V_{\text{OUT}} = -\frac{1}{R_3C_1} \int_0^t V_{\text{IN}} \, dt
\]  

(15-61)

We should point out that Eq. 15-61 assumes that the capacitor is uncharged at \( t = 0 \).

**EXAMPLE 15-26**

Given the op amp inverting integrator shown in Fig. 15-45(a), find the equation for \( V_{\text{OUT}} \). Then assume that \( V_{\text{IN}} \) is \(-10 \text{ mV}\), and find \( V_{\text{OUT}} \) at 0.1 s and at 0.2 s. The integrator’s output voltage is initially zero. How long will it take the integrator’s output to saturate?

**SOLUTION** Since \( R_3 \) is 10 k\( \Omega \), and \( C_1 \) is 0.1 \( \mu \text{F} \), we see that

\[
    V_{\text{OUT}} = -\frac{V_{\text{IN}}}{R_3C_1} t = -\frac{V_{\text{IN}}}{(10 \text{ k}\Omega)(0.1 \text{ \mu F})} t = -1000V_{\text{IN}} t
\]

If \( V_{\text{IN}} \) is \(-10 \text{ mV}\) and \( t \) is 0.1 s,

\[
    V_{\text{OUT}} = -1000V_{\text{IN}} t = -(1000)(-10 \text{ mV})(0.1 \text{ s}) = 1 \text{ V}
\]

and in 0.2 s,

\[
    V_{\text{OUT}} = -1000V_{\text{IN}} t = -(1000)(-10 \text{ mV})(0.2 \text{ s}) = 2 \text{ V}
\]

Assuming that \( +V_{\text{SAT}} \) is 13 V, we may solve for the time to reach saturation.

\[
    V_{\text{OUT}} = \frac{V_{\text{IN}}}{R_3C_1} t = +V_{\text{SAT}}
\]

\[
    t = \frac{+V_{\text{SAT}}}{-V_{\text{IN}}} \frac{R_3C_1}{13 \text{ V}} = \frac{13 \text{ V}}{-(10 \text{ mV})} (10 \text{ k}\Omega)(0.1 \text{ \mu F})
\]

\[
    = (1300)(1 \text{ ms}) = 1.3 \text{ s}
\]

The integrator’s output has been sketched in Fig. 15-45(d).

Now that we understand the noninverting comparator and the inverting integrator, let us analyze a practical op amp triangle generator. One such circuit is given in Fig. 15-46(a).
Assume that the output of the comparator is negative. Its constant negative output level will cause the integrator to ramp in a positive direction. When the output of the integrator becomes positive enough (equal to \( V_{\text{UTP}} \)), the comparator’s output will switch to its positive value. Its constant positive output level will cause the integrator’s output to ramp in a negative direction. As the integrator’s output ramps down from \( V_{\text{UTP}} \), it will eventually reach \( V_{\text{LTP}} \). When this occurs the comparator’s output will switch back to its negative output level, and the cycle repeats. The waveforms have been shown in Fig. 15-46(b).

\[\text{FIGURE 15-46 Practical triangle-waveform generator: (a) circuit; (b) output waveforms } f_0 = 2.05 \text{ kHz}; (c) integrator’s output.\]
Now we determine the formula for the frequency of oscillation of the triangle generator [see Fig. 15-46(c)]. The output of the integrator ramps down from the $V_{\text{UTP}}$ to the $V_{\text{LTP}}$ and then back to the $V_{\text{UTP}}$. From the figure we see that

$$V_{\text{UTP}} = \frac{R_1}{R_2} (V_Z + 0.7 \text{ V})$$

and

$$V_{\text{LTP}} = -\frac{R_1}{R_2} (V_Z + 0.7 \text{ V})$$

The output of the comparator is clamped by a pair of back-to-back zener diodes. The output of the comparator is the "$V_{\text{IN}}$" of the integrator. Hence

$$V_{\text{IN}} = V_Z + 0.7 \text{ V}$$

and this positive input voltage causes the output of the integrator to ramp in a negative direction from $V_{\text{UTP}}$. The equation that describes the integrator’s output voltage is

$$v_{\text{OUT}} = V_{\text{UTP}} - \frac{V_{\text{IN}}}{R_3 C_1} t$$

If we substitute in our equations for $V_{\text{UTP}}$ and $V_{\text{IN}}$, we arrive at the following result:

$$v_{\text{OUT}} = V_{\text{UTP}} - \frac{V_{\text{IN}}}{R_3 C_1} t = \frac{R_1}{R_2} (V_Z + 0.7 \text{ V}) - \frac{V_Z + 0.7 \text{ V}}{R_3 C_1} t$$

The time $t_1$ is the time required for $v_{\text{OUT}}$ to ramp down to the lower trigger point.

$$v_{\text{OUT}} = \frac{R_1}{R_2} (V_Z + 0.7 \text{ V}) - \frac{V_Z + 0.7 \text{ V}}{R_3 C_1} t_1 = V_{\text{LTP}}$$

After substituting in our relationship for $V_{\text{LTP}}$, we may solve for $t_1$.

$$\frac{R_1}{R_2} (V_Z + 0.7 \text{ V}) - \frac{V_Z + 0.7 \text{ V}}{R_3 C_1} t_1 = -\frac{R_1}{R_2} (V_Z + 0.7 \text{ V})$$

Dividing both sides by $(V_Z + 0.7 \text{ V})$, we can then easily solve for $t_1$.
\[
\frac{R_1}{R_2} - \frac{t_1}{R_3C_1} = \frac{R_1}{R_2} - \frac{2R_1}{R_2} = \frac{2R_1R_3C_1}{R_2}
\]

By inspection of Fig. 15-46(c), we can see that \(t_1\) is equal to \(t_2\), and that their sum yields the period \(T\). The reciprocal of the period produces the frequency.

\[
T = t_1 + t_2 = 2t_1 = \frac{4R_1R_3C_1}{R_2}
\]

\[
f_o = \frac{1}{T} = \frac{R_2}{4R_1R_3C_1}
\]

where \(f_o\) is the frequency of oscillation of the op amp triangle generator.

**EXAMPLE 15-27**

Find the frequency of oscillation of the op amp triangle generator given in Fig. 15-46(a). Also determine the peak-to-peak voltage of the square wave, and the peak-to-peak voltage of the triangle wave.

**SOLUTION** From Eq. 15-62,

\[
f_o = \frac{R_2}{4R_1R_3C_1} = \frac{820 \text{ k}\Omega}{(4)(100 \text{ k}\Omega)(10 \text{ k}\Omega)(0.1 \text{ \mu} \text{F})} = 2.05 \text{ kHz}
\]

(Both the triangle wave and the square wave will have the same frequency.) The peak-to-peak voltage of the square-wave output is set by the zener diodes at 19.6 V peak to peak. The triangle wave will have a peak-to-peak output voltage that is equal in magnitude to the hysteresis of the comparator. Thus

\[
u_{\text{OUT}(P-P)} = H = V_{\text{UTP}} - V_{\text{LTP}} = 2 \frac{R_1}{R_2} (V_z + 0.7 \text{ V})
\]

\[
= 2 \frac{100 \text{ k}\Omega}{820 \text{ k}\Omega} (9.1 \text{ V} + 0.7 \text{ V}) = 2.4 \text{ V}
\]

The values have been labeled on Fig. 15-46(b).

**PROBLEMS**

Drill, Derivations, and Definitions

**Section 15-1**

15-1. In your own words, explain the basic differences between amplifiers and oscillators.
15-2. What are the two basic categories of oscillator circuits? Explain their differences.