10-22 Sketch the circuit of an \( P^2L \) inverter. Explain the operation of the circuit and compare it to a resistor-transistor inverter.

10-23 Sketch \( P^2L \) NAND and NOR gates and explain how they operate.

10-24 Using illustrations, explain the construction of an \( P^2L \) circuit, and discuss its advantages compared to other logic types.

10-25 Compare the various types of IC logic in terms of propagation delay time, power dissipation, noise immunity, and fan-out.

INTRODUCTION

A sampling gate is a switching circuit which usually is employed to sample the amplitude of dc or low-frequency signals. Sampling gate circuits can be constructed using diodes, bipolar transistors, or FETs. For large signal voltages, diodes or bipolar transistors may be satisfactory. For very small signals, JFETs or MOSFETs produce the best results.

11-1 DIODE SAMPLING GATE

A very simple diode gate which may be applied to voltage level sampling is shown in Figure 11-1. The signal \( V_s \) to be sampled is applied to the cathode of \( D_1 \). The output voltage \( V_o \) is derived from the cathode of \( D_2 \). A pulse control input \( V_t \) is applied via \( R_1 \) to the anodes of \( D_1 \) and \( D_2 \). The signal source resistance is \( R_s \), and the load is \( R_L \). When the control voltage is zero or negative, diodes \( D_1 \) and \( D_2 \) are reverse-biased, and \( V_o \approx 0 \) V. When the control voltage becomes positive, \( D_1 \) and \( D_2 \) are forward-biased. Then,

\[
V_A = V_s + I_s R_s
\]
It is seen that the signal voltage is passed to the output terminals when the control voltage pulses positively. The waveforms of input voltage, control voltage, and output voltage are illustrated in Figure 11-1(b). The circuit shown can sample only positive input signals. Reversing the diodes and the control input would permit sampling of a negative signal voltage.

The diode sampling gate has errors due to differences in the voltage drops across each diode, and due to diode leakage currents. Consequently, diode gates are applicable only where large signal amplitudes are involved and where accuracy is not important.

11-2  BIPOLAR TRANSISTOR SERIES GATE

The circuit of a bipolar transistor series sampling gate is shown in Figure 11-2. The low-frequency signal to be sampled is applied to the collector, and the output is derived from the emitter terminal. A pulse waveform at the base acts as a control, driving the transistor into saturation and cutoff. When the control voltage is positive, $Q_1$ is biased on. When the control voltage goes to zero, $Q_1$ is off. At transistor saturation, the output voltage is $V_o \approx V_s$. At cutoff, the output becomes zero. It is seen that the transistor is operating as a switch, and that the output from the gate is a series of samples of the input amplitude.

The waveforms in Figure 11-2 are drawn for a positive input signal. If the input becomes negative, as shown in Figure 11-3(a), then the transistor operates in the inverted mode. The emitter terminal acts as the collector, and the collector operates as the transistor emitter. This, by no means, is an efficient way to operate a transistor used for amplification. However, as a saturated switch with a large base current, the transistor performs satisfactorily in inverted mode. To ensure that the device will switch off, the negative swing of the control voltage must be greater than the negative...
The input signal applied to a sampling gate is frequently a very low level voltage. Since the transistor saturation voltage constitutes a loss of signal amplitude [see Figure 11-4(a)], \( V_{CE(qn)} \) (also termed the offset voltage) must be maintained as small as possible. Reference to the transistor characteristics in Figure 4-2 shows that for the smallest \( V_{CE(qn)} \), \( I_c \) must be kept small and \( I_B \) must be relatively large. For \( I_C = 1 \) mA and \( I_B = 0.1 \) mA, a typical \( V_{CE(qn)} \) is 0.2 V. Another source of error is the emitter-base leakage current \( I_{EO} \) that flows when the device is biased off. \( I_{EO} \) causes an unwanted output voltage to develop across load resistance \( R_L \) [see Figure 11-4(b)]. A typical level of \( I_{EO} \) for a switching transistor is 50 mA at 25°C.

In the design of a series sampling gate, the load resistance \( R_L \) should be selected much larger than the signal source resistance \( R_s \). This will avoid large signal currents which would cause a significant voltage drop across \( R_s \). The signal current can be reduced to a minimum if \( I_B \) is made equal to the output current \( I_F \). The amplitude of the control voltage should be greater than the peak signal voltage. The sampling frequency (i.e., the control voltage frequency) should be several times the frequency of the signal to be sampled.

**EXAMPLE 11-1**

Design a transistor series gate to sample a signal with a peak amplitude of 2 V, and a source resistance of 100 Ω. Also calculate the output errors due to \( V_{CE(qn)} \) and \( I_{EO} \).
solution

\[ R_L \gg R_s \]

Let

\[ R_L = 100 \times R_s = 100 \times 100 \, \Omega = 10 \, k\Omega \]

When the transistor is on,

\[ V_o = V_s \]

\[ I_o = \frac{V_s}{R_L} = \frac{2 \, V}{10 \, k\Omega} = 200 \, \mu A \]

Let

\[ I_B = I_o = 200 \, \mu A \]

The control voltage \( V_1 > V_s \).

Let

\[ V_1 = 2 \times V_s = 2 \times 2 \, V = 4 \, V \]

\[ I_B = \frac{V_1 - V_{BE} - V_s}{R_B} \]

200 \, \mu A = \frac{4 \, V - 0.7 \, V - 2 \, V}{R_B}

and

\[ R_B = \frac{1.3 \, V}{200 \, \mu A} = 6.5 \, k\Omega \]

(use 6.8 \, k\Omega standard value)

Typically, \( V_{CE(sat)} = 0.2 \, V \), and \( I_{EO} = 50 \, nA \).

Error due to \( V_{CE(sat)} \)

\[ \frac{V_{CE(sat)}}{V_s} \times 100\% = \frac{0.2 \, V}{2 \, V} \times 100\% = 10\% \]

Error due to \( I_{EO} \)

\[ \frac{(I_{EO} R_L)}{V_s} \times 100\% = \frac{50 \, nA \times 10 \, k\Omega}{2 \, V} \times 100\% \]

= 0.025\%

Sec. 11-3  BIPOLAR TRANSISTOR SHUNT GATE

11-3  BIPOLAR TRANSISTOR SHUNT GATE

The series sampling gate is suitable for signals having a low source resistance. For signals with a very high source resistance, the series gate requirement that \( R_L \) be much larger than \( R_s \) is difficult to fulfill. In this case, a shunt sampling gate is most suitable.

In the shunt sampling gate (Figure 11-5), transistor \( Q_1 \) shorts the input to ground when it is switched into saturation. When \( Q_1 \) is off, current flows

(a) Shunt gate circuit

(b) Current and voltage waveforms

FIGURE 11-5.  Bipolar transistor shunt gate and waveforms.
from the signal source to the load resistance. Therefore, the shunt sampling gate essentially is a current switch, whereas the series sampling gate is a voltage switch. The transistor offset voltage results in a load current \( V_{CE(on)} / R_L \) when the transistor is on [Figure 11-6(a)]. When the device is off, some of the signal current is lost as \( I_{CO} \) through the transistor [Figure 11-6(b)]. If the input signal becomes negative, the transistor operates in the inverted mode, as in the case of the series gate.

The load resistance for a shunt sampling gate should be selected such that \( I_O R_L \) is much larger than \( V_{CE(on)} \). For transistor saturation and for minimum \( V_{CE(on)} \), \( I_B \) can be approximately equal to \( I_O \). As in the case of the series gate, the sampling frequency should be at least several times the signal frequency. The transistor leakage current \( I_{CO} \) should be very much smaller than \( I_O \).

**EXAMPLE 11.2**

Design a transistor shunt gate to sample a signal current having a peak amplitude of 2 mA. Also, calculate the output errors due to \( V_{CE(on)} \) and \( I_{CO} \).

---

Section 11.3 **BIPOLAR TRANSISTOR SHUNT GATE**

solution

\( I_O \approx I_s = 2 \text{ mA} \)

Let

\[
I_O R_L = 10 \times V_{CE(sat)}
\]

\[
R_L = \frac{10 \times V_{CE(sat)}}{I_O} = \frac{10 \times 0.2 \text{ V}}{2 \text{ mA}} = 1 \text{ k}\Omega
\]

Let

\( I_B \approx I_O = 2 \text{ mA} \)

Take

\[
V_I = 4 \text{ V}
\]

\[
I_B = \frac{V_I - V_{BE}}{R_B} = \frac{4 \text{ V} - 0.7 \text{ V}}{2 \text{ mA}} = 1.65 \text{ k}\Omega \quad \text{(use 1.8 k}\Omega \text{ standard value)}
\]

\[
R_B = \frac{3.3 \text{ V}}{2 \text{ mA}} = 1.65 \text{ k}\Omega
\]

Error current due to \( V_{CE(on)} = \frac{V_{CE(sat)}}{R_L} \)

Error due to \( V_{CE(sat)} = \frac{V_{CE(sat)} / R_L}{I_O} \times 100\% \)

\[
= \frac{0.2 \text{ V} / 1 \text{ k}\Omega}{2 \text{ mA}} \times 100\% = 10\%
\]

Typical \( I_{CO} = 50 \text{ nA} \)

Error due to \( I_{CO} = \frac{I_{CO}}{I_O} \times 100\% \)

\[
= \frac{50 \text{ nA}}{2 \text{ mA}} \times 100\% = 0.0025\%
\]
11-4 JFET SERIES GATE

A series sampling gate using an n-channel JFET is shown in Figure 11-7. Note that the control voltage $V_t$ goes from $+V_t$ to a negative level greater than the transistor pinchoff voltage $V_p$. When $V_t = +V_p$, the FET is on. When $-V_t > V_p$, the device is off. Note that because the drain terminal of the FET goes up to $+V_t$, the gate must also go up to that level for $Q_3$ to be correctly biased on. A gate resistance $R_g$ (typically 1 MΩ) is usually included to limit any gate current that might flow. The JFET can also be operated in inverted mode, in which case the drain terminal acts as a source, and the source terminal performs the function of the drain. Inverted operation of a JFET is satisfactory only if the signal level is very small. If the signal becomes large, the (inverted) gate-channel junction could become forward-biased, and the resultant gate current would affect the drain-source voltage.

Field effect transistors have a drain-source voltage drop of $I_D R_{D(on)}$ when biased into saturation [see Figure 11-7(b) and Sec. 4-5]. With small drain current, this drain-source voltage drop can be much smaller than the $V_{CEO}$ of a bipolar transistor. A typical value of $R_{D(on)}$ for a switching FET is 30 Ω, although devices with $R_{D(on)}$ as low as 5 Ω are available. For a load current of 200 μA, as in Example 11-1, the typical FET offset voltage is $(200 \mu A \times 30 Ω) = 6$ mV. This is only 0.3% of a 2 V signal, compared to the 10% loss due to the $V_{CEO}$ of the bipolar transistor. When the JFET is biased off there is a gate-source leakage current $I_{GSS}$, which corresponds to $I_{ESO}$ in a bipolar transistor [Figure 11-7(c)]. Thus, $I_{GSS}$ constitutes an unwanted load current. For a switching JFET $I_{GSS}$ can be 0.2 nA or less, which is superior to the typical 50 nA of a bipolar device. The performance specification for some switching JFETs is given below:

<table>
<thead>
<tr>
<th>Maximum pinchoff voltage</th>
<th>Drain-source on resistance $R_{D(on)}$</th>
<th>Gate-source leakage $I_{GSS}$</th>
<th>Drain-source leakage $I_{D(on)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2N4391</td>
<td>10 V</td>
<td>30 Ω</td>
<td>0.1 nA</td>
</tr>
<tr>
<td>2N5433</td>
<td>9 V</td>
<td>7 Ω</td>
<td>0.2 nA</td>
</tr>
</tbody>
</table>

Note that the data sheet for the 2N4391 is in Appendix 1-10.

EXAMPLE 11-3

A low-frequency signal with a peak amplitude of 1 V is applied to a voltage follower with a very low output resistance. The signal is to be sumed together with a 12 V voltage. The output voltage is

\[ V_O = V_S + 12 \]
solved at the output of the voltage follower and fed to a circuit with $R_t = 10 \text{k}\Omega$. Design a suitable FET gate circuit and estimate the output errors.

**Solution**

The circuit is as shown in Figure 11-8. For the 2N4391 FET, the control voltage $V_t > (V_{P(on)} = 10 \text{V})$. Let

$$V_t = -12 \text{V}$$

With $Q_1$ on,

$$I_D \approx \frac{V_t}{R_s + R_t} \
= \frac{1 \text{V}}{0 \text{V} + 10 \text{k}\Omega} = 0.1 \text{mA}$$

$$V_{DS(on)} = I_D R_{D(on)} = 0.1 \text{mA} \times 30 \text{\Omega} = 3 \text{mV}$$

Error due to $V_{DS(on)} = \frac{V_{DS(on)}}{V_t} \times 100\%$

$$= \frac{3 \text{mV}}{1 \text{V}} \times 100\% = 0.3\%$$

With $Q_1$ off,

$$I_o = I_{GSS} = 0.1 \text{nA}$$

$$V_o = I_{GSS} R_t = 0.1 \text{nA} \times 10 \text{k}\Omega = 1 \text{\muV}$$

Error due to $I_{GSS} = \frac{I_{GSS} R_t}{V_t} \times 100\%$

$$= \frac{1 \text{\muV}}{1 \text{V}} \times 100\% = 0.001\%$$

### 11-5 JFET SHUNT GATE

The JFET shunt sampling gate shown in Figure 11-9(a) operates in a similar way to the bipolar shunt circuit. Like the bipolar shunt gate, the JFET shunt gate is essentially a current switch. When the FET is on, the output of the gate is shorted to ground. The output voltage at this time actually is $I_D R_{D(on)}$, and this produces an unwanted output current ($I_D R_{D(on)} / R_L$) [see Figure 11-9(b)]. However, for the shunt FET gate, the unwanted output is much less than the minimum possible with a bipolar circuit. When the transistor is off, the drain-source leakage current $I_{D(ult)}$ diverts signal current from the load [see Figure 11-9(c)]. Again, this usually is less than the corresponding bipolar leakage current.

**EXAMPLE 11-4**

A low-frequency current with an amplitude of 0.1 mA is to be sampled and fed to the input of a circuit with $R_t = 10 \text{k}\Omega$. Design a suitable FET shunt gate, and estimate the output voltage errors due to the transistor.
solution

Use a 2N4391 FET. Let the control voltage be $-12\,\text{V}$ as in Example 11-3. When $Q_1$ is on,

$$V_o = I_s R_{D\text{(on)}} = 0.1\,\text{mA} \times 30\,\Omega = 3\,\text{mV}$$

and when $Q_1$ is off,

$$V_o = I_s R_i = 0.1\,\text{mA} \times 10\,\text{k}\Omega = 1\,\text{V}$$

The error when $Q_1$ is on is given by

$$\frac{3\,\text{mV} \times 100}{1\,\text{V}} = 0.3\%$$

when $Q_1$ is off.

$$I_D = I_{D\text{(off)}} = 0.1\,\text{nA}$$

$$I_o = I_s - I_{D\text{(off)}} = 0.1\,\text{mA} - 0.1\,\text{nA}$$

Error = $\frac{0.1\,\text{nA} \times 100}{0.1\,\text{mA}} = 0.0001\%$

---

11-6 MOSFET SAMPLING GATES

MOSFETs are almost ideal devices for use as sampling gates. They have the same low $R_{D\text{(on)}}$ characteristic as JFETs, and the enhancement mode devices are normally off while the gate is at the same potential as the substrate. Figure 11-10(a) shows the circuit of a series sampling gate using an $n$-channel MOSFET. With the substrate at ground potential, the control voltage should go from 0 V to a positive voltage to switch the gate from off to on. When the input signal can be either negative or positive, the substrate should be taken to a negative bias voltage and the control voltage should start at the bias level. A MOSFET shunt sampling gate is shown in Figure 11-10(b). Here, again, the substrate terminal of the FET can be taken to a negative bias voltage, and the control voltage should start at the bias level to accommodate negative signal voltages.

FIGURE 11-10. MOSFET sampling gate.
The circuit in Figure 11-10(c) is a series gate employing two MOSFETs. This circuit is particularly suitable where the load has a very high input resistance. When \( Q_1 \) is on, the signal voltage is switched to the load, and \( Q_2 \) is off. When \( Q_1 \) is off, the load voltage should be zero. With \( Q_2 \) on at this time, the output voltage is

\[
(I_{D(on)} \text{ for } Q_1) \times (R_{D(on)} \text{ for } Q_2)
\]

When typical values of 0.1 nA and 30 Ω are used, the unwanted output voltage is only 3 nV.

One problem in using MOSFETS as sampling gates is that the control voltage (applied to the gate) must always be greater than the maximum signal level. In fact, the control voltage must usually exceed the maximum signal amplitude by at least 2 V. Since there is very little voltage drop along the channel of the FET, both drain and source terminals are closely equal to the signal voltage level (as desired). Therefore, the channel of the device is always at the same potential as the signal. If the signal approaches the level of the control voltage, there may not be sufficient gate-channel bias to properly turn the device on. Thus, part of the signal may not be reproduced accurately at the output. The CMOS transmission gate overcomes this difficulty.

As shown in Figure 11-11, a CMOS transmission gate consists of two complementary MOSFETs connected in inverse parallel. The drain of \( Q_1 \) is connected to the source terminal of \( Q_2 \), and the source of \( Q_1 \) is connected to the drain of \( Q_2 \). Both substrate terminals are grounded, and each gate has its own control voltage.

Note that the control voltage waveforms in Figure 11-11 show that the \( n \)-channel device \( Q_1 \) has a control voltage which goes from ground to a positive voltage level. \( Q_2 \), the \( p \)-channel FET, has a control voltage that goes from ground to a negative level. Note also that the two control waveforms are in antiphase. When \( Q_1 \) gate is positive, the gate of \( Q_2 \) is driven negative. This means that both devices are turned on and off simultaneously. Both present a low resistance path from input to output when on, and both offer a high resistance between input and output when off.

Now consider the signal and output waveforms illustrated in Figure 11-11. The input amplitude is shown as ± 8 V, and the control voltage on \( Q_1 \) gate is +8 V, while that to \( Q_2 \) is −8 V. During the time that the signal is positive, current can flow from input to output along both FET channels when the devices are biased on. If the positive amplitude of the signal approaches the control voltage amplitude (as illustrated), \( Q_1 \) tends to switch off, because there is not sufficient gate-channel voltage difference to keep it biased on. However, \( Q_2 \) is not affected, because its gate-channel

11-7 OPERATIONAL AMPLIFIER SAMPLING GATE

An operational amplifier connected as an inverting amplifier can be made into a sampling gate by installing a FET across its feedback resistor. The
As with other sampling gates, the output waveform is a series of instantaneous samples of the input. However, in this case the output samples are an inverted version of the input. Also, the input can be amplified in the sampling process, depending upon the selection of the ratio \( R_2 / R_1 \). When \( Q_1 \) is an n-channel JFET, as illustrated, its control voltage should go down to a negative level equal to the FET maximum pinch-off voltage to ensure switch off, and up to ground level for switch on. When a MOSFET is employed, the required control voltage levels are as discussed in Sections 11-4 and 11-5.

Because of the use of an operational amplifier, this gate has a very low output impedance. Its input impedance is equal to \( R_1 \). Design procedure for the gate simply involves designing an inverting amplifier and selection of a suitable FET.

**EXAMPLE 11-5**

A sampling gate using a 741 operational amplifier and a 2N4391 FET is to have a voltage gain of 10. The maximum signal voltage is \( V_s = 500 \text{ mV} \). Select suitable resistor values and control voltage amplitude. Also estimate the output error due to the \( R_{D(oo)} \) of the FET.

**solution**

for the 741, \( I_{R(max)} = 500 \text{ nA} \)

let

\[
I_1 = 100 \times I_{R(max)} = 100 \times 500 \text{ nA} = 50 \mu\text{A}
\]

\[
R_1 = \frac{V_s}{I_1} = \frac{500 \text{ mV}}{50 \mu\text{A}} = 10 \text{ k} \Omega \quad \text{(standard value)}
\]

\[
R_2 = A_v R_1 = 10 \times 10 \text{ k} \Omega = 100 \text{ k} \Omega \quad \text{(standard value)}
\]

*Note that for a precise gain of 10, \( R_1 \) and \( R_2 \) would have to be precision resistors.*

\[
R_3 = R_1 || R_2 \approx 10 \text{ k} \Omega
\]

for the 2N4391, \( V_{P(max)} = 10 \text{ V} \) (see Appendix 1-10). Therefore, the control
voltage is, \( V_1 > 10 \) V

\[
R_{D(oh)} = 30 \, \Omega
\]

Zero output = \( V_s \times \frac{R_{D(oh)} || R_2}{R_1} \)

\[
= 500 \, \text{mV} \times \frac{30 \, \Omega || 100 \, \text{k}\Omega}{10 \, \text{k}\Omega} = 1.5 \, \text{mV}
\]

\[
V_s = \frac{R_2}{R_1} \times V_s
\]

= 10 \times 500 \, \text{mV}

= 5 \, \text{V}

Zero error = \( \frac{1.5 \, \text{mV}}{5 \, \text{V}} \times 100\% = 0.03\% \)

### 11-8 SAMPLE-AND-HOLD CIRCUIT

A sample-and-hold circuit, as its name implies, samples the instantaneous amplitude of a signal, and then holds the output voltage constant until the next sampling instant. The circuit, see Fig. 11-13(a), is simply a series gate with a capacitor \( C_1 \) to perform the holding function. Operational amplifiers \( A_1 \) and \( A_2 \) are connected as voltage followers (see Section 7-7) to provide high input impedance and low output impedance.

The waveforms in Figure 11-13(a) illustrate the relationship between input and output. At time \( t_a \), the instantaneous amplitude of the input is \( v_s \). The output holds at the \( v_s \) level until time \( t_b \), when it jumps to the input amplitude \( v_s \). Similarly, when the input is falling, the output amplitude remains constant at \( v_s \) from \( t_b \) to \( t_c \).

During the sampling time \( t_1 \), \( Q_1 \) is on and \( C_1 \) is charged via \( R_{D(oh)} \), as illustrated in Figure 11-13(b). If the sampling time is

\[
t_1 = 5 \, CR
\]

where \( R \) is \( R_{D(oh)} \),

the capacitor is charged to 0.993 of the input voltage. (This comes from Equation 2.2.) Allowing the capacitor to charge to 0.993 of \( V_s \) results in a 0.7% error in the sampled amplitude. If \( t = 7 \, CR \), \( V_s = 0.999 \, V_s \), i.e., a 0.1% error.

During the holding time \( t_2 \), \( C_1 \) is partially discharged by the bias current \( I_{S2} \) flowing into \( A_2 \). The FET source-gate leakage current \( I_{GS} \) also

---

**Figure 11-13.** Sample-and-hold circuit.
causes some discharge of $C_1$. However, $I_{Q5}$ is normally very much less than $I_{B2}$, so it can usually be neglected. The capacitance of $C_1$ is calculated from the knowledge of $I_{B2}$, the holding time $t_2$, and the acceptable error due to $C_1$ discharge. After the value of $C_1$ is established, the sampling time $t_1$ is calculated from $C_1$ and the acceptable charging error.

One more source of error in the output voltage is the FET gate-source capacitance $C_{GS}$. When the control voltage on the gate goes to its lowest level, $C_{GS}$ is charged to $e_c=(V_s+V_i)$. [This is illustrated in Figure 11-13(c)]. The charge on $C_{GS}$ is removed from $C_1$, and thus reduces $V_0$. Example 11-6 demonstrated how a sample-and-hold circuit is designed, and how the various error sources affect the accuracy of the sample.

EXAMPLE 11-6

A sample-and-hold circuit is to use 741 operational amplifiers and a 2N4391 FET. The signal voltage amplitude, $V_s=\pm 1$ V, is to be sampled with an accuracy of approximately 0.25%. The holding time is 500 $\mu$s. Determine the capacitor value and the minimum sampling time. Also calculate the effect of $C_{GS}=10.5$ pF.

solution

for the 741, $I_{B(max)}=500$ nA. Allow $I_{B(max)}$ to discharge $C_1$ by 0.1% during $t_2$.

\[
\Delta V = 0.1\% \text{ of } 1 \text{ V} = 1 \text{ mV}
\]

\[
C_1 = \frac{I_B \times t_2}{\Delta V} = \frac{500 \text{ nA} \times 500 \mu\text{s}}{1 \text{ mV}} = 0.25 \mu\text{F}
\]

for the 2N4391, $R_D(\text{on})=30 \Omega$. Allow another 0.1% error in $V_s$ due to the sampling time $t_1$.

For 0.1% error, $t_1 = 7 \times C \times R_D(\text{on})$

\[
= 7 \times 0.25 \mu\text{F} \times 30 \Omega = 52.5 \mu\text{s}
\]

\[V_1 = -[V_s(max) + V_{spok}] = -[10 \text{ V} + 1 \text{ V}] = -11 \text{ V} \]

Effect of $C_{GS}=10.5$ pF:

\[V_{GS(max)} = +V_s - V_1 = 1 \text{ V} - (-11 \text{ V}) = 12 \text{ V} \]

charge on $C_{GS}$ is $Q=C_{GS} \times V_{GS(max)}$

\[= 10.5 \text{ pF} \times 12 \text{ V} = 150 \text{ pC} \]

when $Q$ is removed from $C_1$,

\[\Delta V_s = \frac{Q}{C_1} = \frac{150 \text{ pC}}{0.25 \mu\text{F}} = 600 \mu\text{V} \]

% error due to $C_{GS}$

\[
\frac{\Delta V_s}{V_s} \times 100\% = \frac{600 \mu\text{V}}{1 \text{ V}} \times 100\% = 0.06\%
\]

REVIEW QUESTIONS AND PROBLEMS

11-1 Sketch the circuit of a diode sampling gate. Show the voltage waveforms, explain the operation of the circuit, and discuss the error sources.

11-2 Repeat Problem 11-1 for a bipolar transistor series sampling gate.

11-3 Explain how a bipolar transistor series sampling gate functions when the input signal is alternately positive and negative with respect to ground.

11-4 Design a bipolar transistor series gate to sample a signal with a