Agenda

• Virtex™-II Overview

• Virtex-II Design Solutions
  – Active Interconnect™ Technology
  – Clock Management
  – Memory Hierarchy
  – I/Os Standard
  – Configuration/Data Security
  – Packages

• Conclusion
Virtex-II Platform FPGA Solution

SelectI/O+™ Technology:
Leading-Edge I/O Standards

Enhanced SelectRAM+™ Hierarchy

Data Security

Data Storage

Data Processing

Full Supported by ISE 4.2i and leading Synthesis tools

IP-Immersion Platform for Mega-Density Designs

High Performance with Ease of Use

XILINX APD APPS, 02/02 3
Virtex-II Architecture
Agenda

• Virtex-II Overview

• Virtex-II Architecture
  – Active interconnect technology
  – Clock management
  – I/O standards
  – Memory hierarchy
  – Configuration/data security
  – Packages

• Conclusion
Active Interconnect Technology

- Interconnect an array of switch matrices
- All Virtex II features can access routing resources through the switch matrix
  - Simplify design and place & route

Switch Matrix ↔ CLB

Switch Matrix ↔ IOB

Switch Matrix ↔ DCM

Switch Matrix ↔ 18Kb BRAM

MULT 18x18
CLB Contains Four Slices

- Each CLB is connected to one switch matrix
  - Providing access to general routing resources

High level of logic integration
- Wide-input functions:
  - 16:1 multiplexer in 1 CLB or any function
  - 32:1 multiplexer in 2 CLBs (1 level of LUT)
- Fast arithmetic functions
  - 2 look-ahead carry chains per CLB column
- Addressable shift registers in LUT
  - 16-b shift register in 1 LUT
  - 128-b shift register in 1 CLB (dedicated shift chain)
Horizontal Cascade Chain

- Wide AND-OR functions (Sum Of Products)
CLB Multiplexers

CLB Multiplexer Location

MUXF8 combines the 2 MUXF7 outputs (Two CLB)

MUXF6 combines Slices X1Y0 & X1Y1

MUXF7 combines the 2 MUXF6 outputs

MUXF6 combines Slices X0Y0 & X0Y1
Shift Register Look-Up Table

- High density integration of shift registers
  - DSP applications use SRL16 for delay matching
  - CDMA wireless and video applications require shift registers

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>✅</td>
<td>Up to 128-b per CLB</td>
</tr>
<tr>
<td>✅</td>
<td>Cascadable output</td>
</tr>
<tr>
<td>✅</td>
<td>Dynamic addressable output</td>
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<tr>
<td>✅</td>
<td>16-b per LUT</td>
</tr>
</tbody>
</table>

Multiple SRLC16 cascadable to any length
Sophisticated Digital Clock Manager

- High-Speed 420 MHz clock generation:
  - Clock de-skew on-chip and off-chip

<table>
<thead>
<tr>
<th>Feature</th>
<th>Status</th>
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<tr>
<td>Up to 12 DCM per device</td>
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<tr>
<td>Fully digital circuitry</td>
<td>✔</td>
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<tr>
<td>Flexible Frequency Synthesis</td>
<td>✔</td>
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<tr>
<td>Synthesis outputs: clock 0° &amp; 180° (def.: 4X)</td>
<td>✔</td>
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<tr>
<td>High-Resolution Phase Shifting</td>
<td>✔</td>
</tr>
<tr>
<td>DPS fixed and variable modes</td>
<td>✔</td>
</tr>
<tr>
<td>Delay-Locked Loop (DLL)</td>
<td>✔</td>
</tr>
<tr>
<td>Precise Clock De-Skew</td>
<td>✔</td>
</tr>
<tr>
<td>DLL outputs: clock 0°, 90°, 180°, 270°</td>
<td>✔</td>
</tr>
<tr>
<td>DLL outputs: clock 2X and clock division</td>
<td>✔</td>
</tr>
<tr>
<td>50/50 duty cycle correction</td>
<td>✔</td>
</tr>
</tbody>
</table>
Digital Clock Manager: DCM

Delay-Locked Loop
- Clock phase de-skew
- Duty cycle correction
- Temperature compensation
- RST input
- LOCKED output
- Attributes:
  - DUTY_CYCLE_CORRECTION
  - DLL_FREQUENCY_MODE
  - CLKDV_DIVIDE = 1.5 to 16.0
  - STARTUP_WAIT
  - CLK_FEEDBACK = CLK0 or CLK2X
- Up to 4 clock outputs per DCM
Advanced Frequency Synthesis

DCM

- Frequency Synthesis
  - CLKFX is any M / D product of CLKIN frequency
  - M = 2 to 32, D = 1 to 32
  - Default: M=4, D=1 (4X CLKIN)
  - Always nominal 50/50 duty-cycle
- Attributes:
  - CLKFX_MULTIPLY (integer)
  - CLKFX_DIVIDE (integer)
  - DFS_FREQUENCY_MODE

After LOCKED: $\text{Freq}_{\text{CLKFX}} = \frac{M}{D} \times \text{Freq}_{\text{CLKIN}}$

Clock signal
Control signal
High Resolution Phase Shifting

Fine Phase Shifting
- Applies to all CLK outputs
- Phase shift = fraction CLKin period
- Fixed or variable modes
- Inputs in variable mode:
  - PSINCDEC input = Increase / Decrease
  - PSEN = Enable Phase Shift
  - PSCLK synchronizes Phase Shift
- PSDONE output
- Attributes:
  - CLOCKOUT_PHASE_SHIFT = NONE, FIXED, VARIABLE
  - PHASE_SHIFT (signed integer)
    -255 to +255
Phase Shift Effects

Note: for frequencies below 90 MHz, the minimum tap is approximately 45 ps in all cases.
Global Clocks

- Up to 16 Dedicated Low Skew Clocks

| ✔️ 16 global clock multiplexers & buffers |
| ✔️ 8 clock nets in each quadrant |
| ✔️ Global clock ENABLE |
| ✔️ Switch glitch-free from one clock to another |
| ✔️ 16 clock pads (can be used as user I/O) |
Enhanced Clock Distribution

• 16 Global Clock Multiplexers
  – Eight on the top
  – Eight on the bottom
  – Switch “glitch free” from 1 clock to the other

• 8 Clocks selectable per quadrant

Unused Branches are Disable (Power Saving)
Global Clocks: BUFGMUX

- Three modes:
  - Clock buffer
    - Low skew clock distribution
    - BUFG primitive
  - Clock enable
    - Stop the clock High or Low
    - BUFGCE (stop Low)
  - Clock multiplexer “glitch-free”
    - Switch from one clock to another
    - BUFGMUX
    - unrelated clocks

No pulse width shorter than 1/2 of the period
Memory Bandwidth and Flexibility

Enhanced On-Chip SelectRAM™ Memory

- DSP Coefficients
- Small FIFOs
- CAM
- Shallow/Wide

- Large FIFOs
- Packet Buffers
- Video Line Buffers
- Cache Tag Memory
- CAM
- Deep/Wide

- 128x1
- 18 kb Blocks
- Up to 400 Mbps/pin
- DDR & QDR

Distributed RAM

Block RAM

External RAM/CAM

Terabit Memory Continuum
Embedded 18 kb Block RAM

- Up to 3 Mb on-chip block RAM
- High internal buffering bandwidth
- Reduced I/O count and more embedded memory

| ✔ 18Kbit block RAM |
| ✔ Parity bit locations (parity in/out busses) |
| ✔ Data width up to 36 bits |
| ✔ 3 WRITE modes |
| ✔ Output latches Set/Reset |
| ✔ True Dual-Port RAM |
| ✔ Independent clock (async.) & control |
True Dual-Port™ Configurations

Configurations available on each port:

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Depth</th>
<th>Data bits</th>
<th>Parity bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>16K x 1</td>
<td>16Kb</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>8K x 2</td>
<td>8Kb</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>4K x 4</td>
<td>4Kb</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>2K x 9</td>
<td>2Kb</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>1K x 18</td>
<td>1Kb</td>
<td>16</td>
<td>2</td>
</tr>
<tr>
<td>512 x 36</td>
<td>512</td>
<td>32</td>
<td>4</td>
</tr>
</tbody>
</table>

- Independent port A and B configuration:
  - Support for data width conversion including parity bits
New BRAM Write Modes

- Each port supports 3 “WRITE” modes set by configuration
  - “WRITE_FIRST” mode: Output latches = Input bus
    - Data_in → DI Internal Memory → DO
      DO = Data_in
  - “READ_FIRST” mode: Output latches = Memory Data
    - Data_in → DI Internal Memory → DO
      DO = prior stored data
  - “NO_CHANGE” mode: Output latches are frozen
    - Data_in → DI Internal Memory → DO
      DO (no change during Write)
SelectRAM+ Distributed RAM

- Virtex-II LUT can implement:
  - 16 x 1-bit synchronous RAM
  - Synchronous write
  - Asynchronous read
    - D flip-flop in the same slice can register the output
- Can cascade 8 LUTs in a CLB to form 128-bit wide
- Allow fast embedded RAM of any width
  - Only limited by the number of slices in each device
  - Example: RAM 64 x 12-bit fits in 48 LUTs
New 18 x 18 Embedded Multiplier

- Fast arithmetic functions
  - Optimized to implement multiply / accumulate modules

<table>
<thead>
<tr>
<th></th>
<th>18 x 18 signed multiplier</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Fully combinatorial</td>
</tr>
<tr>
<td></td>
<td>Optional registers with CE &amp; RST (pipeline)</td>
</tr>
<tr>
<td></td>
<td>Independent from adjacent block RAM</td>
</tr>
</tbody>
</table>
18 x 18 Multiplier

- Embedded 18-bit x 18-bit multiplier
  - 2’s complement signed operation
- Multipliers are organized in columns

Note: See Virtex-II Data Sheet for updated performances
Select I/O-Ultra™ Technology

- High Bandwidth and XCITE™ on-chip termination
  - Support 19 single-ended standards and 6 differential standards

| ✔ | Digitally controlled impedance (XCITE) |
| ✔ | Up to 840 Mbps per I/O pair (LVDS) |
| ✔ | Built-in DDR registers |
| ✔ | LVDS current source drivers |
| ✔ | LDT & ULVDS differential signaling |
| ✔ | HSTL-II standard support |
| ✔ | Up to 1,108 user I/Os |
High-Speed Interface Design

• Leading edge FPGA I/O performance at 840 Mbps
• Support latest hot communication interface protocols, including:
  – PCI-X 133 MHz
  – RapidI/O™ support
  – POS PHY Level 4 (16 bits/clk @ 832 Mbps), SPI-4
  – Lightening Data Transport (LDT) support
Up to 1108 User I/Os

- Double data rate
  - Input, output and 3-state control registers
- Up to 554 differential I/O pairs:
  - High-speed LVDS, Bus LVDS, and LVPECL on all I/O pairs
- Single-ended I/O: 19 standards supported
  - PCI @ 33 MHz & 66 MHz compliant
  - PCI-X @ 133 MHz compliant
  - LVTTL, LVCMOS, SSTL, HSTL, GTL, AGP
IOB: Double Data Rate Registers

• DDR registers can be clocked by
  – Clock and not (clock) if the duty cycle is 50/50
  – CLK0 and CLK180 DLL outputs
IOB Element

- Input path
  - Two DDR registers
- Output path
  - Two DDR registers
  - Two 3-state DDR registers
- Separate clocks for I & O
- Set and reset signals are shared
  - Separated sync/async
  - Separated Set/Reset attribute per register
Differential Signaling, up to 840 Mbps

- **LVDS**: Low-Voltage Differential Signal
  - Current source drivers
- **Bus LVDS**: bidirectional LVDS communication
- **LVPECL**: Low-Voltage Positive Emitter Coupler Logic
  - ~850 mV voltage swing
LVDS Implementation

• Full LVDS Programmable Solution:
  • 2.5 V : 250 mV - 400 mV
  • 3.3 V : 250 mV - 400 mV
  • Ext. 2.5 V : 350 mV - 750 mV
  • Ext. 3.3 V : 350 mV - 750 mV

• Current driver
Digitally Controlled Impedance

• Dynamically adjusted termination resistors
  – Provides drivers that matched to the impedance of the traces
  – Provides on-chip termination
  – Transmitter or receiver

• On-Chip termination advantages:
  – No termination resistors on board
  – Improve signal integrity by eliminating stub reflection
  – Eliminates the need for source termination (single-ended I/O)
  – Reduces board routing headaches and component count
Digitally Controlled Impedance

- **DCI** and **DCI_DV2**
  - Low voltage CMOS with adjustable impedance
  - 3.3V, 2.5V, 1.8V and 1.5V
  - Two reference resistors per bank
    - With 1% R, the impedance is in +/- 10% range
    - Range: 25 ohms to 150 ohms (Advanced info)
  - **DCI_DV2** is adjusted to half of the reference resistor.

![Digitally Controlled Impedance Diagram](image-url)
DCI I/O Standards

• Driver
  – LVDCI_15
  – LVDCI_18
  – LVDCI_25
  – LVDCI_33
  – LVDCI_DV2_15
  – LVDCI_DV2_18
  – LVDCI_DV2_25
  – LVDCI_DV2_33

• Termination
  – GTL_DCI
  – GTLP_DCI
  – HSTL_I_DCI
  – HSTL_II_DCI
  – HSTL_III_DCI
  – HSTL_IV_DCI
  – SSTL2_I_DCI*
  – SSTL2_II_DCI*
  – SSTL3_I_DCI*
  – SSTL3_II_DCI*

* SSTL compatible
Virtex-II Configuration

• SRAM-based in-system configuration
  – Slave and master serial modes
  – Slave and master SelectMAP mode
    • Fast 8-bit parallel configuration
  – Built-In IEEE 1532 support
  – Partial reconfiguration capability
  – Readback capability for real-time debugging

• Built-In Internal Logic Analyzer (ILA)
  – Complete solution for access and verification
Virtex-II Family: Two Columns
Block RAM & Multipliers Devices

Low density, all features, high performances devices

- XC2V40
- XC2V80
Virtex-II Family: Four and Six Columns Block RAM & Multiplier Devices

XC2V250
# Virtex-II Family Members

<table>
<thead>
<tr>
<th>Device XC2V</th>
<th>40</th>
<th>80</th>
<th>250</th>
<th>500</th>
<th>1000</th>
<th>1500</th>
<th>2000</th>
<th>3000</th>
<th>4000</th>
<th>6000</th>
<th>8000</th>
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<tbody>
<tr>
<td>CLB Array</td>
<td>8</td>
<td>16</td>
<td>24</td>
<td>32</td>
<td>40</td>
<td>48</td>
<td>56</td>
<td>64</td>
<td>80</td>
<td>96</td>
<td>112</td>
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<tr>
<td>18Kb BRAM</td>
<td>4</td>
<td>8</td>
<td>24</td>
<td>32</td>
<td>40</td>
<td>48</td>
<td>56</td>
<td>96</td>
<td>120</td>
<td>144</td>
<td>168</td>
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<tr>
<td>Multiplier</td>
<td>4</td>
<td>8</td>
<td>24</td>
<td>32</td>
<td>40</td>
<td>48</td>
<td>56</td>
<td>96</td>
<td>120</td>
<td>144</td>
<td>168</td>
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<tr>
<td>DCM</td>
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<td>4</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
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<tr>
<td>Max IOB</td>
<td>88</td>
<td>120</td>
<td>200</td>
<td>264</td>
<td>432</td>
<td>528</td>
<td>624</td>
<td>720</td>
<td>912</td>
<td>1,104</td>
<td>1,296</td>
</tr>
</tbody>
</table>

- 2 Columns: BRAM & Multipliers
- 4 Columns: BRAM & Multipliers
- 6 Columns: BRAM & Multipliers
Virtex II Packaging

• Wire-bond packages

• Flip-chip packages
  – Higher device I/O count
  – Higher thermal capacity

• Ball-grid arrays:
  – FGxxx: wire-bond fine-pitch BGA (1.00 mm pitch)
  – BGxxx: wire-bond BGA (1.27 mm pitch)
  – FFxxx: flip-chip fine-pitch BGA (1.00 mm pitch)
  – BFxxx: flip-chip BGA (1.27 mm pitch)
Flip-Chip Packaging: Best Thermals & Small Package

- Better electrical performance due to improved supply voltage distribution to core
- Dissipate up to 30 watts
- 2X more I/Os than SBGA
- Higher frequency switching with better noise control
## Virtex-II Packaging

<table>
<thead>
<tr>
<th>Device XC2V</th>
<th>40</th>
<th>80</th>
<th>250</th>
<th>500</th>
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<th>2000</th>
<th>3000</th>
<th>4000</th>
<th>6000</th>
<th>8000</th>
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<tbody>
<tr>
<td>Max user I/Os</td>
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<td>120</td>
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<td>264</td>
<td>432</td>
<td>528</td>
<td>624</td>
<td>720</td>
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<td>684</td>
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<td>684</td>
</tr>
</tbody>
</table>

- FF and BF are flip-chip ball grid arrays packages
- Pinout compatibility inside same color rectangle
Agenda:

• Virtex™-II Overview
• Virtex-II Design Solutions
• Conclusion
Xilinx 1st Platform FPGA solution designed for ease of performance:

- 0.15\(\mu\) 8LM Copper CMOS Process, with 0.12 \(\mu\) Transistors
- IP-Immersion™ Architecture
- Upward compatible with Virtex, Virtex-E Devices
- 3x increase in capacity to 10M systems gates
- 1.5X increase in speed to 200MHz+ System Clock
- Dynamic on-chip termination and impedance matching
- Sophisticated DCM for high-speed clock design
- I/O bandwidth @ 840 Mbps
  - Integrated RapidI/O, LDT, PCI-X, POS PHY Level 4 support
- Best memory to logic ratio
  - Highest internal RAM bandwidth