Computer Bus Structures

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Introduction

- **Concept of the basic bus**
- **Description of available Internal bus Systems**
- **Description of available External bus systems**

Basic Bus

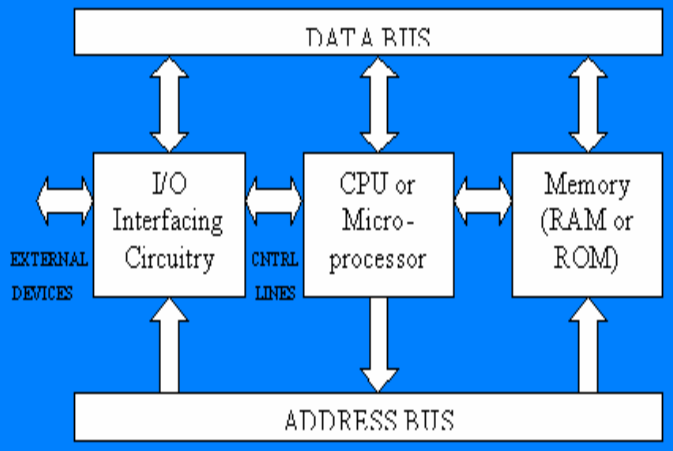
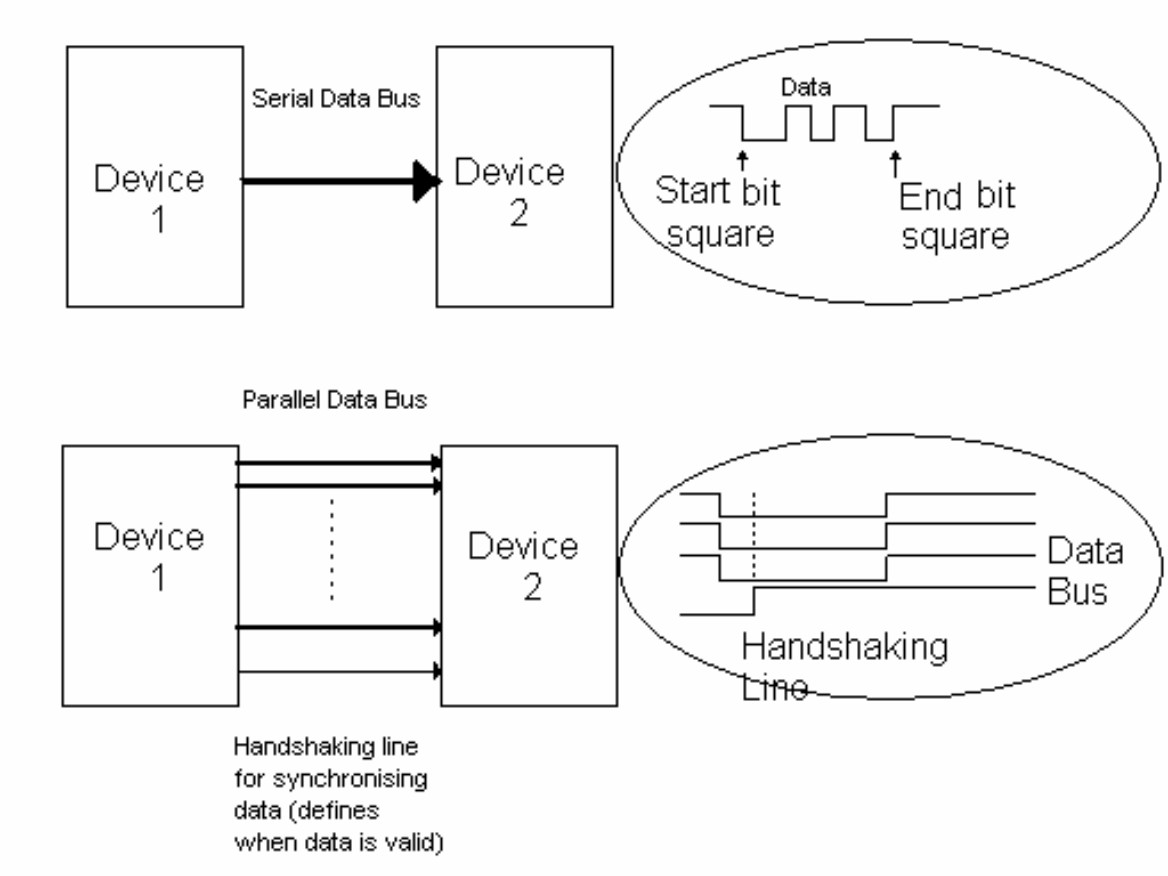


Figure 1: Block diagram of a basic computer system.

- **Data bus**
- **Address bus**
- **Handshaking lines**
- **Control lines**

Data Bus

- **Function of a data bus is to send data from one device to another**
- **Data is passed in parallel or serial manner**
  - **Parallel will normally pass in a multiple of 8-bits at a time**
  - **Serial passes one bit at a time**



- **Parallel data bus is faster**
- **Parallel data bus requires an extra handshaking line to synchronize the data transfer**

Address Bus

- e.g. CPU needs to read an instruction (data) from a given location in memory
- Identify the source or destination of data
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

Addressable memory in bytes/address bus size	
Address Bus Size	Addressable memory (bytes)
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1K
11	2K
12	4K
13	8K
14	16K

Data Handshaking Lines

- **Critical for the flow of orderly data**

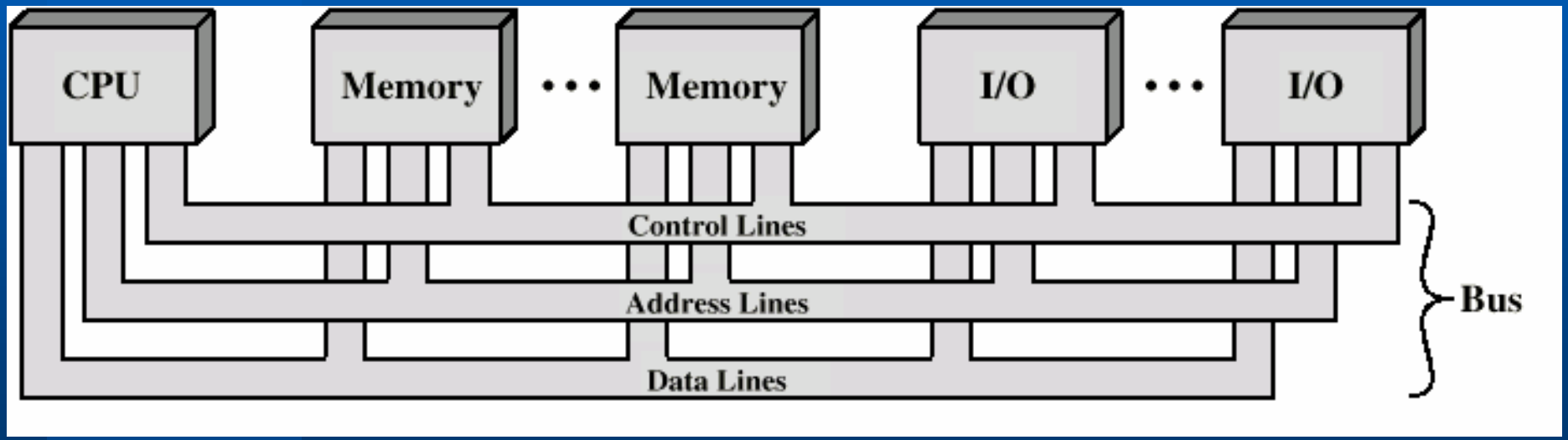
- **Basic Handshaking consists of two lines:**
  - **-Sending identification line**
  - **-Receiving identification line**

Control Lines

- Controls the access to the data and address lines
- Controls the use of the data and address lines
- Typical control lines include the following:

- Memory write
- Memory read
- I/O write
- I/O read
- Transfer ACK
- Bus request
- Bus grant
- Interrupt request
- Interrupt ACK
- Clock
- Reset

BUS Interconnection Scheme



Bus Type

- **Dedicated**
  - **Separate data & address lines**
- **Multiplexed**
  - **Shared lines**
  - **Address valid or data valid control line**
  - **Advantage - fewer lines**
  - **Disadvantages**
    - **More complex control**
    - **Ultimate performance**

Bus Arbitration

- More than one module controlling the bus
- e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed

Method of Arbitration

Centralized

- **Single hardware device controlling bus access**
  - **Bus Controller**
  - **Arbiter**
- **May be part of CPU or separate**

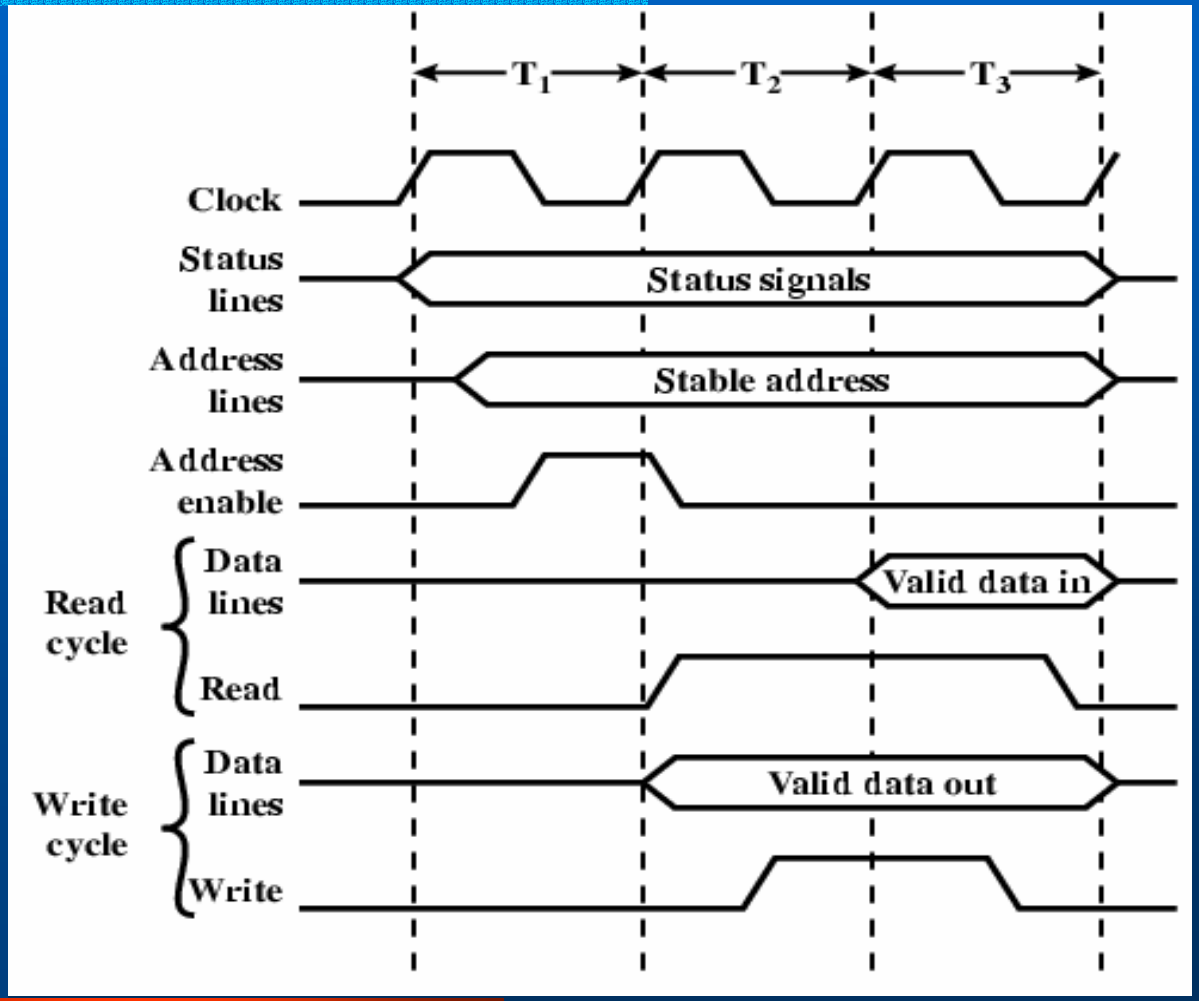
Distributed

- **Each module may claim the bus**
- **Control logic on all modules**

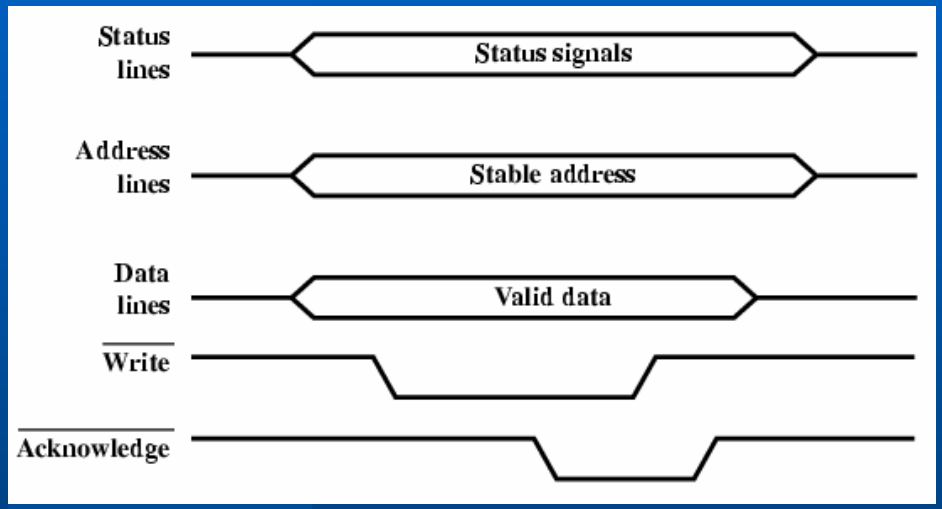
Timing

- Co-ordination of events on bus
- Synchronous
  - Events determined by clock signals
  - Control Bus includes clock line
  - A single 1-0 is a bus cycle
  - All devices can read clock line
  - Usually sync on leading edge
  - Usually a single cycle for an event
- Asynchronous
  - Occurrence of one event on a bus depends on previous events

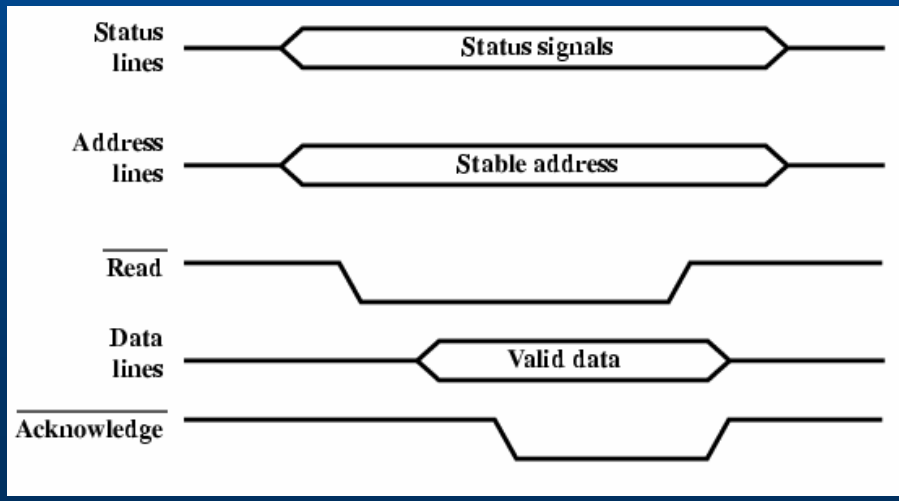
Synchronous Timing Diagram



Asynchronous Timing



Write cycle



Read cycle

Bus Width

- **Wider data bus = Greater number of bits at one time**
- **Wider address bus = Greater range of locations that can be referenced**

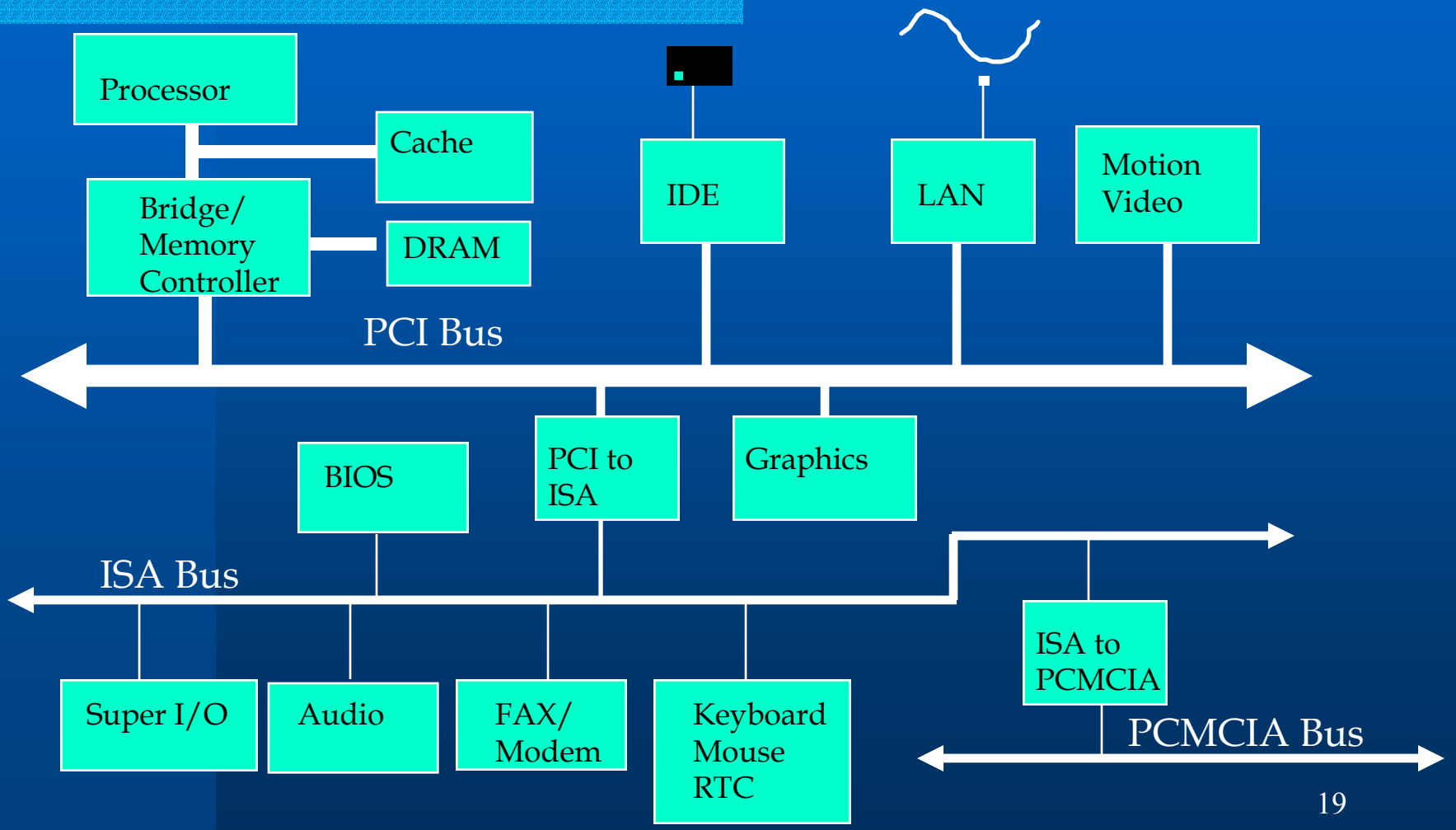
Busses Covered

INTERNAL BUSSES		EXTERNAL BUSSES	
Parallel	**Serial**	**Parallel**	**Serial**
S-100	I2C	ATA	ACCESS BUS
ISA	SPI	IEEE-488	ADB
EISA	Hiper Transport	HIPPI	Fibre Channel
MCA	PCI-EXPRESS	PCMCIA	IEEE-1394
NUBUS		SCSI	RS-422 & RS-485
SBUS			Serial ATA
PCI			SSA
VME			USB
VESA			CAN

PCI

- Peripheral Component Interconnection
- An example of an internal parallel bus
- High bandwidth
- Intel released to public domain
- 32 or 64 bit
- 50 lines @ 66 MHz
- Transfer Rate of 528MB/s

System of Today



PCI Bus Lines Required

- Systems lines
  - Including clock and reset
- Address & Data
  - 32 time mux lines for address/data
  - Interrupt & validate lines
- Interface Control
- Arbitration
  - Not shared
  - Direct connection to PCI bus arbiter
- Error lines

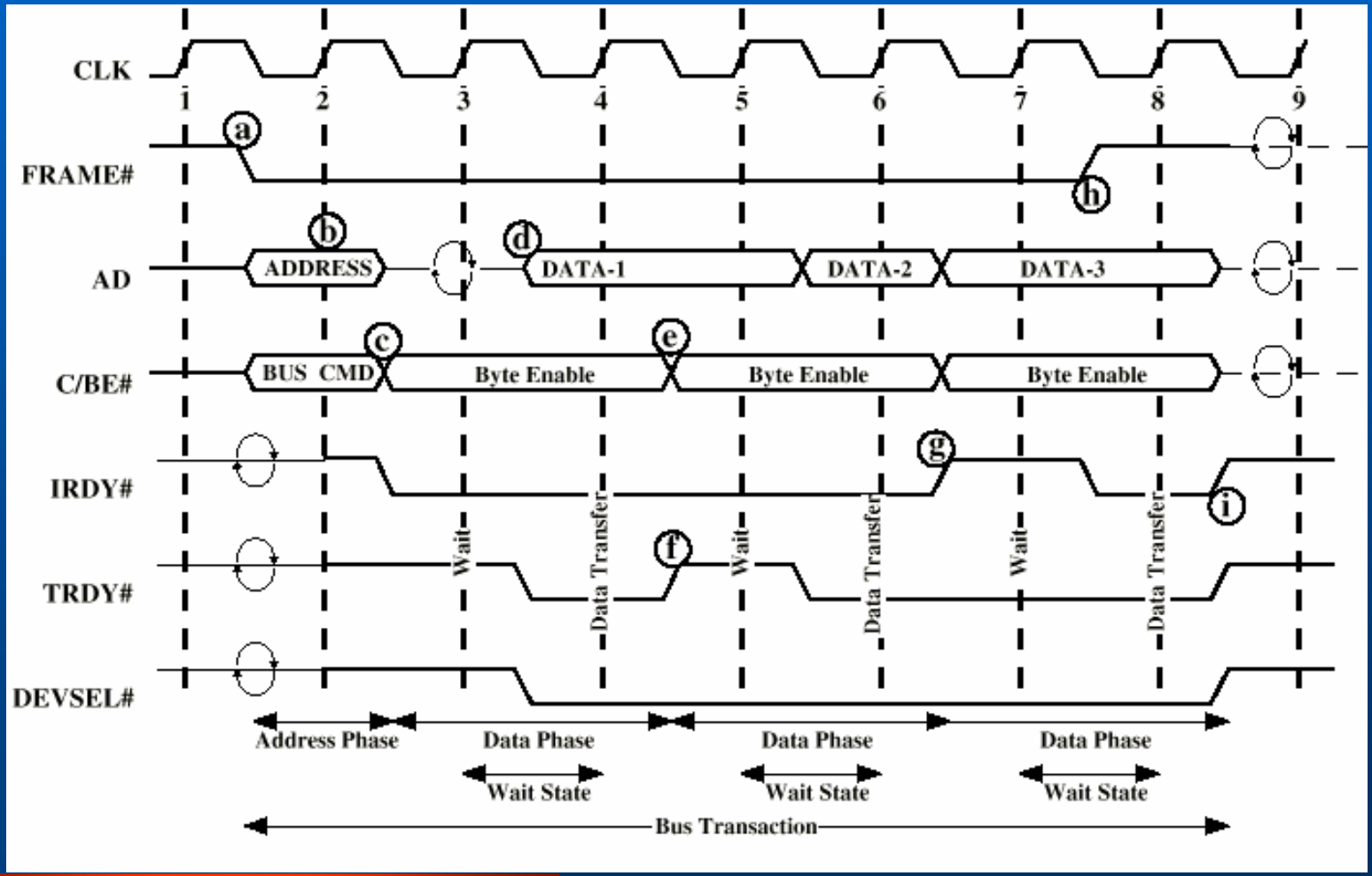
Optional PCI Bus Lines

- **Interrupt lines**
  - **Not shared**
- **Cache support**
- **64-bit Bus Extension**
  - **Additional 32 lines**
  - **Time multiplexed**
  - **2 lines to enable devices to agree to use 64-bit transfer**
- **JTAG/Boundary Scan**
  - **For testing procedures**

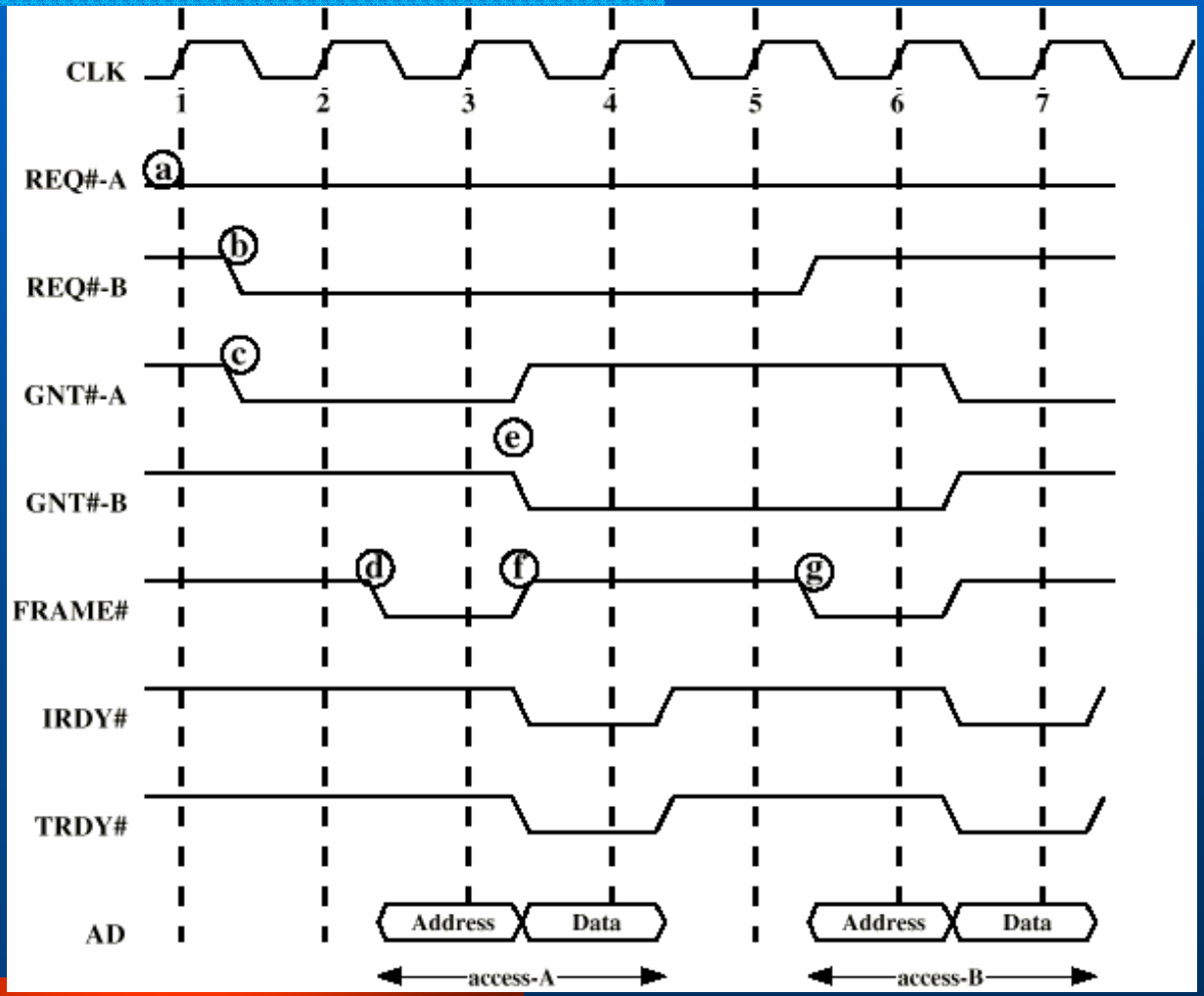
PCI Commands

- Transaction between initiator (master) and target
- Master claims bus
- Determine type of transaction
  - e.g. I/O read/write
- Address phase
- One or more data phases

PCI Read Timing Diagrams

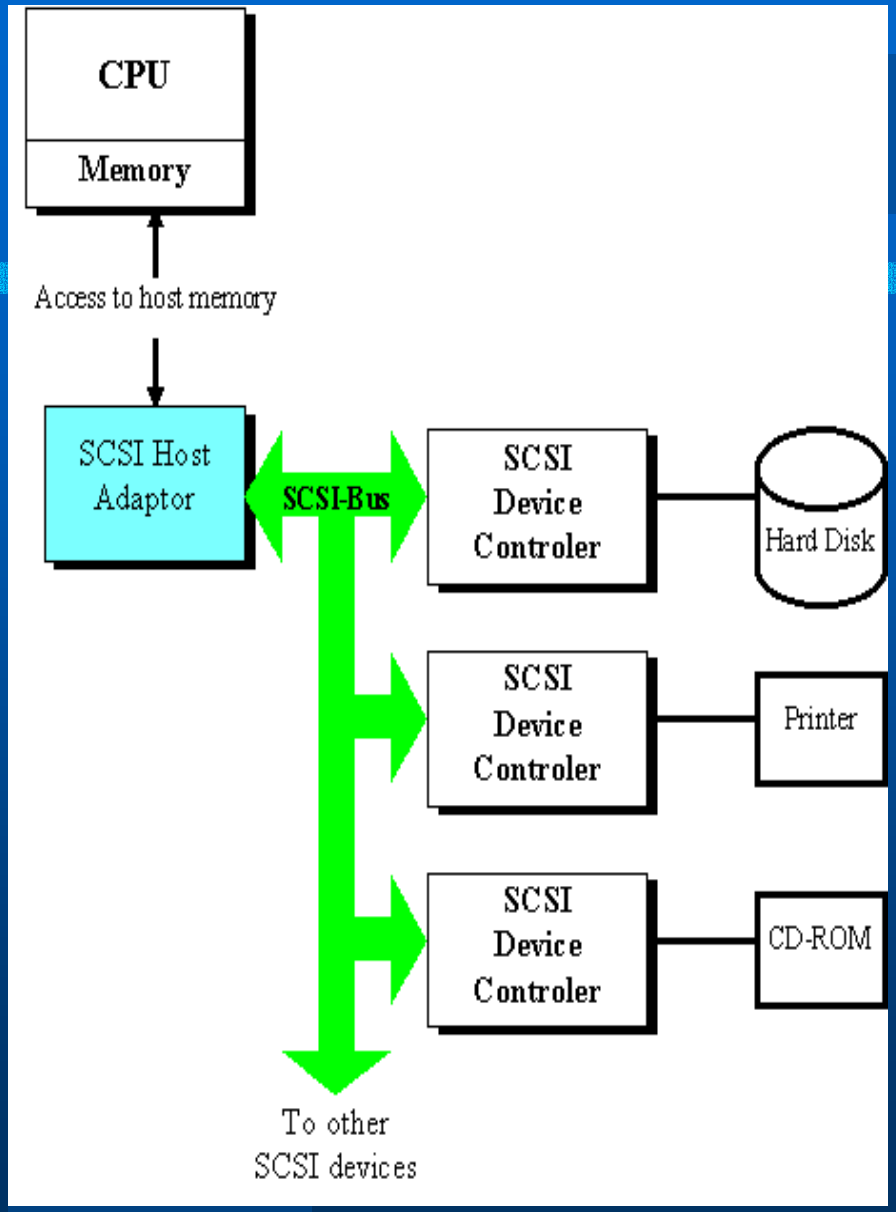


Bus Arbitration



SCSI

- **Small Computer System Interface.**
- **A high-speed, intelligent peripheral I/O bus with a device independent protocol. It allows different peripheral devices and hosts to be interconnected on the same bus. Depending on the type of SCSI, you may have up to 8 or 16 devices connected to the SCSI bus.**



- There must be at least one initiator (usually a host) and one target (a peripheral device) on a bus.
- There is a large variety of peripheral devices available for SCSI, including hard disk drives, floppy drives, CDs, optical storage devices, tape drives, printers and scanners to name a few.

SCSI Bus Phases

- **BUS Free Phase**
  - **BUS FREE phase begins when the SEL and BSY signals are both continuously false for a bus settle delay. It ends when the BSY signal becomes true.**
- **Arbitration Phase**
  - **In this state a unit can take control of the bus and become an initiator.**

SCSI Bus Phases (cont'd)

- **Selection Phase**
  - **In this state the initiator selects a target unit and gets the target to carry out a given function, such as reading or writing data.**

SCSI Bus Phases (cont'd)

- **Message Phase**
  - **This is the first information transfer phase in the connection. It allows the initiator to send an Identify message to the target. Messages are always transferred asynchronously**

SCSI Bus Phases (cont'd)

- **Command Phase**
  - **The command phase is used by the target to request command information from the initiator.**
- **Data In Phase**
  - **The target responds with Inquiry data. The data is transferred synchronously if both the target and the initiator have previously established a synchronous data transfer agreement**

SCSI Bus (cont'd)

- **Status Phase**
  - **The target sends a single status byte asynchronously**
- **Message In Phase**
  - **The last information that is transferred in the connection is typically the Command Complete message**
- **Back to Bus Free Phase**

Varieties of SCSI

- SCSI-1
- SCSI-2
- Wide SCSI
- Fast SCSI
- Fast Wide SCSI
- Ultra SCSI
- SCSI-3
- Ultra2 SCSI
- Wide Ultra2 SCSI

SCSI vs. ATA (IDE, EIDE)

- **SCSI does not utilize the CPU for data transfer management.**
- **SCSI is more expensive than EIDE**
- **SCSI can handle more devices**

Fibre Channel

- **Fibre Channel is an open T11 and ANSI standards-based block-oriented serial network protocol that brings together some of the best features of the channel world and the network world.**
- **Fibre Channel is full-duplex (Full duplex means that data can travel in both directions simultaneously.), and offers a variety of different cabling options.**

Advantages

- **Cost-effective – it is cost effective for storage and networks**
- **Reliable – it is reliable with assured information delivery**
- **Gigabit bit rate – 1.06 Gbps, scalable to 2.12 Gbps and 4.24 Gbps**
- **Multiple topologies – it has dedicated point-to-point, shared loops, and scaled switched topologies meet application requirements**

Advantages (cont'd)

- **Multiple protocols – it supports SCSI, TCP/IP, video, or raw data , and is especially suited to real-time video/audio.**
- **Scalable – it supports single point-to-point gigabit links to integrated enterprises with hundreds of servers.**
- **Congestion Free – data can be sent as fast as the destination buffer can receive it.**

Advantages (cont'd)

- **High Efficiency – fibre channel has very little transmission overhead**