Computer Bus Structures

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Introduction

- Concept of the basic bus
- Description of available Internal bus Systems
- Description of available External bus systems
Basic Bus

- Data bus
- Address bus
- Handshaking lines
- Control lines

Figure 1: Block diagram of a basic computer system
Data Bus

- Function of a data bus is to send data from one device to another
- Data is passed in parallel or serial manner
  - Parallel will normally pass in a multiple of 8-bits at a time
  - Serial passes one bit at a time
- Parallel data bus is faster
- Parallel data bus requires an extra handshaking line to synchronize the data transfer
Address Bus

- e.g. CPU needs to read an instruction (data) from a given location in memory
- Identify the source or destination of data
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

<table>
<thead>
<tr>
<th>Address Bus Size</th>
<th>Addressable memory (bytes)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
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<tr>
<td>2</td>
<td>4</td>
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<tr>
<td>3</td>
<td>8</td>
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<td>4</td>
<td>16</td>
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<td>5</td>
<td>32</td>
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<td>6</td>
<td>64</td>
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<tr>
<td>7</td>
<td>128</td>
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<tr>
<td>8</td>
<td>256</td>
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<tr>
<td>9</td>
<td>512</td>
</tr>
<tr>
<td>10</td>
<td>1K</td>
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<tr>
<td>11</td>
<td>2K</td>
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<tr>
<td>12</td>
<td>4K</td>
</tr>
<tr>
<td>13</td>
<td>8K</td>
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<tr>
<td>14</td>
<td>16K</td>
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Data Handshaking Lines

- Critical for the flow of orderly data

- Basic Handshaking consists of two lines:
  - Sending identification line
  - Receiving identification line
Control Lines

- Controls the access to the data and address lines
- Controls the use of the data and address lines
- Typical control lines include the following:
  - Memory write
  - Memory read
  - I/O write
  - I/O read
  - Transfer ACK
  - Bus request
  - Bus grant
  - Interrupt request
  - Interrupt ACK
  - Clock
  - Reset
BUS Interconnection Scheme
Bus Type

- **Dedicated**
  - Separate data & address lines

- **Multiplexed**
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance
Bus Arbitration

- More than one module controlling the bus
- e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed
Method of Arbitration

Centralized
- Single hardware device controlling bus access
  - Bus Controller
  - Arbiter
- May be part of CPU or separate

Distributed
- Each module may claim the bus
- Control logic on all modules
Timing

- Co-ordination of events on bus
- Synchronous
  - Events determined by clock signals
  - Control Bus includes clock line
  - A single 1-0 is a bus cycle
  - All devices can read clock line
  - Usually sync on leading edge
  - Usually a single cycle for an event
- Asynchronous
  - Occurrence of one event on a bus depends on previous events
Asynchronous Timing

Write cycle

Read cycle
Bus Width

- **Wider data bus = Greater number of bits at one time**

- **Wider address bus = Greater range of locations that can be referenced**
# Busses Covered

<table>
<thead>
<tr>
<th>INTERNAL BUSSES</th>
<th>EXTERNAL BUSSSES</th>
</tr>
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<tbody>
<tr>
<td><strong>Parallel</strong></td>
<td><strong>Serial</strong></td>
</tr>
<tr>
<td>S-100</td>
<td>I2C</td>
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<tr>
<td>ISA</td>
<td>SPI</td>
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<td>EISA</td>
<td>Hiper Transport</td>
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<tr>
<td>MCA</td>
<td>PCI-EXPRESS</td>
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<td></td>
<td>ACCESS BUS</td>
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<tr>
<td></td>
<td>ADB</td>
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<tr>
<td></td>
<td>Fibre Channel</td>
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<tr>
<td></td>
<td>IEEE-1394</td>
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<td></td>
<td>RS-422 &amp; RS-485</td>
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<td>Serial ATA</td>
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<td></td>
<td>SSA</td>
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<td>USB</td>
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<td>CAN</td>
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PCI

- Peripheral Component Interconnection
- An example of an internal parallel bus
- High bandwidth
- Intel released to public domain
- 32 or 64 bit
- 50 lines @ 66 MHz
- Transfer Rate of 528MB/s
System of Today

- Processor
- Cache
- DRAM
- Bridge/Memory Controller
- IDE
- LAN
- Motion Video
- BIOS
- PCI to ISA
- Graphics
- Keyboard Mouse RTC
- Super I/O
- Audio
- FAX/Modem
- ISA to PCMCIA
- ISA to ISA
- ISA to PCMCIA Bus
- PCI Bus
- PCMCIA Bus
- ISA Bus
PCI Bus Lines Required

- **Systems lines**
  - Including clock and reset

- **Address & Data**
  - 32 time mux lines for address/data
  - Interrupt & validate lines

- **Interface Control**

- **Arbitration**
  - Not shared
  - Direct connection to PCI bus arbiter

- **Error lines**
Optional PCI Bus Lines

- **Interrupt lines**
  - Not shared

- **Cache support**

- **64-bit Bus Extension**
  - Additional 32 lines
  - Time multiplexed
  - 2 lines to enable devices to agree to use 64-bit transfer

- **JTAG/Boundary Scan**
  - For testing procedures
PCI Commands

- Transaction between initiator (master) and target
- Master claims bus
- Determine type of transaction
  - e.g. I/O read/write
- Address phase
- One or more data phases
PCI Read Timing Diagrams
Bus Arbitration

Diagram showing the timing of various control signals such as CLK, REQ#-A, REQ#-B, GNT#-A, GNT#-B, FRAME#, IREADY#, TREADY#, and AD with control signals for access-A and access-B.
SCSI

- Small Computer System Interface.
- A high-speed, intelligent peripheral I/O bus with a device independent protocol. It allows different peripheral devices and hosts to be interconnected on the same bus. Depending on the type of SCSI, you may have up to 8 or 16 devices connected to the SCSI bus.
There must be at least one initiator (usually a host) and one target (a peripheral device) on a bus.

There is a large variety of peripheral devices available for SCSI, including hard disk drives, floppy drives, CDs, optical storage devices, tape drives, printers and scanners to name a few.
SCSI Bus Phases

- **BUS Free Phase**
  - BUS FREE phase begins when the SEL and BSY signals are both continuously false for a bus settle delay. It ends when the BSY signal becomes true.

- **Arbitration Phase**
  - In this state a unit can take control of the bus and become an initiator.
Selection Phase

- In this state the initiator selects a target unit and gets the target to carry out a given function, such as reading or writing data.
SCSI Bus Phases (cont’d)

- **Message Phase**
  - This is the first information transfer phase in the connection. It allows the initiator to send an Identify message to the target. Messages are always transferred asynchronously
SCSI Bus Phases (cont’d)

- **Command Phase**
  - The command phase is used by the target to request command information from the initiator.

- **Data In Phase**
  - The target responds with Inquiry data. The data is transferred synchronously if both the target and the initiator have previously established a synchronous data transfer agreement.
SCSI Bus (cont’d)

- **Status Phase**
  - The target sends a single status byte asynchronously

- **Message In Phase**
  - The last information that is transferred in the connection is typically the Command Complete message

- **Back to Bus Free Phase**
Varieties of SCSI

- SCSI-1
- SCSI-2
- Wide SCSI
- Fast SCSI
- Fast Wide SCSI
- Ultra SCSI
- SCSI-3
- Ultra2 SCSI
- Wide Ultra2 SCSI
SCSI vs. ATA (IDE, EIDE)

- SCSI does not utilize the CPU for data transfer management.
- SCSI is more expensive than EIDE.
- SCSI can handle more devices.
Fibre Channel

- Fibre Channel is an open T11 and ANSI standards-based block-oriented serial network protocol that brings together some of the best features of the channel world and the network world.

- Fibre Channel is full-duplex (Full duplex means that data can travel in both directions simultaneously.), and offers a variety of different cabling options.
Advantages

- Cost-effective – it is cost effective for storage and networks
- Reliable – it is reliable with assured information delivery
- Gigabit bit rate – 1.06 Gbps, scalable to 2.12 Gbps and 4.24 Gbps
- Multiple topologies – it has dedicated point-to-point, shared loops, and scaled switched topologies meet application requirements
Advantages (cont’d)

- Multiple protocols – it supports SCSI, TCP/IP, video, or raw data, and is especially suited to real-time video/audio.
- Scalable – it supports single point-to-point gigabit links to integrated enterprises with hundreds of servers.
- Congestion Free – data can be sent as fast as the destination buffer can receive it.
Advantages (cont’d)

- High Efficiency – fibre channel has very little transmission overhead