Corporate Overview - 4Q01

- Introduction
- Product Overview
- Strategic Direction
Actel Overview

- Established FPGA Supplier
  - First Product Shipped - 1988
  - $226M in sales in 2000, 32% growth over 1999
  - Strong balance sheet - $135M cash, no debt
  - More than 500 employees
  - 16% R&D spending in 2000

- Three FPGA technologies available
  - Antifuse, Flash, SRAM
  - Substantial FPGA patent portfolio (170+)

- Forbes list of “200 Best Small Companies in America”

- Included in S & P Smallcap 600 Index
Actel’s 3-Tier Aerospace Business Model Differentiation

- **Rad Hard**
  - Radiation Survivability Essential
  - Risk vs. cost concern
  - Long Life 10-15 years
  - Mission Failure disastrous
  - Military & Deep Space Missions

- **Rad Tolerant**
  - Radiation Survivability Important
  - Cost vs. risks concern
  - Short Life 5-7 years
  - LEO Satellites

- **Military/Avionics & Other HiRel**
  - Radiation Survivability not critical
  - Generally Mil-Std 883 or Mil-Temp
  - Avionics, munitions, ground based equipment
  - Harsh Industrial Environments

**Key Parameter**
- Total Dose
- SEU Immunity
- Long Lifetime Harsh Environments
Actel Product Spectrum Today

Customer Need

Radiation Hard
- RH

Radiation Tolerant
- RTSX-S

SEU Immunity
- RTAX-S (Planned)

Military/Avionic/HiRel
- ProASIC PLUS
- ProASIC

Harsh Environments
- Harsh Environs
- Long Life

Total Dose
- SEU Immunity
- Total Dose

Density

3,000 10,000 100,000 1M 2M

Customer Need

RH

RTSX-S

RTAX-S (Planned)

ProASIC PLUS

ProASIC

SX-A
## Actel YTD 2001 Revenue Profile

### By Market Segment
- Mil/Aero: 24%
- Communications: 53%
- Industrial/Other: 3%
- Consumer: 1%
- Computing: 1%

### By Geographical Segment
- North America: 61%
- Europe: 29%
- Pan-Asia: 10%
Agenda

- Introduction
- Product Overview
- Strategic Direction
## Antifuse Product Offering

### Benefits of antifuse FPGA technology

- High performance
- Low power
- Single-chip
- Secure
- Live at power-up
- Cost effective

<table>
<thead>
<tr>
<th>Product</th>
<th>Process</th>
<th>K Gates</th>
<th>Max I/O</th>
<th>Leading features</th>
</tr>
</thead>
<tbody>
<tr>
<td>SX-A</td>
<td>0.22um</td>
<td>108</td>
<td>360</td>
<td>Performance, non-volatile features</td>
</tr>
<tr>
<td>eX</td>
<td>0.22um</td>
<td>12</td>
<td>130</td>
<td>1/6 power of typical CPLD (64-256 mcell)</td>
</tr>
<tr>
<td>RTSX-S</td>
<td>0.22um</td>
<td>108</td>
<td>205</td>
<td>SEU immune with built-in TMR</td>
</tr>
<tr>
<td>Express</td>
<td>0.15um</td>
<td>2000</td>
<td>684</td>
<td>Performance, interface features</td>
</tr>
</tbody>
</table>
SX-A Family

- 250 MHz system performance
- Low power
- Single-chip
- Live at power-up
- Hot-swap support
- Mixed-voltage support
  - 2.5V, 3.3V, 5V
- Cost leadership for high-volume apps

<table>
<thead>
<tr>
<th></th>
<th>SX08A</th>
<th>SX16A</th>
<th>SX32A</th>
<th>SX72A</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Gates</td>
<td>12k</td>
<td>24k</td>
<td>48k</td>
<td>108k</td>
</tr>
<tr>
<td>Logic Modules</td>
<td>768</td>
<td>1452</td>
<td>2880</td>
<td>6036</td>
</tr>
<tr>
<td>Registers</td>
<td>256</td>
<td>528</td>
<td>1080</td>
<td>2012</td>
</tr>
<tr>
<td>Max User I/O</td>
<td>130</td>
<td>177</td>
<td>249</td>
<td>360</td>
</tr>
</tbody>
</table>
SX-A Leadership

- Performance leadership versus mainstream competition

![Bar chart showing comparison]

<table>
<thead>
<tr>
<th>Customer Designs</th>
<th>Spartan2-6</th>
<th>SXA-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTL</td>
<td>13</td>
<td>8.2</td>
</tr>
<tr>
<td>INTF960</td>
<td>14.65</td>
<td>11.1</td>
</tr>
<tr>
<td>INT_TOP</td>
<td>16.18</td>
<td>11.9</td>
</tr>
<tr>
<td>MCDATA</td>
<td>14</td>
<td>7.6</td>
</tr>
<tr>
<td>OMC_TOP</td>
<td>14.76</td>
<td>9.2</td>
</tr>
<tr>
<td>CIGABIT2</td>
<td>9.8</td>
<td>8.9</td>
</tr>
<tr>
<td>PHOTOPR</td>
<td>15</td>
<td>11.7</td>
</tr>
<tr>
<td>STSTOP</td>
<td>16</td>
<td>8.2</td>
</tr>
<tr>
<td>FPGA1</td>
<td>11.1</td>
<td>7.9</td>
</tr>
</tbody>
</table>
RTSX-S Family

Features

- Designed specifically for Space Applications
- Up to 2,012 SEU Hardened Flip-Flops eliminate Software TMR Design
- Single EventLatch-up Immune
- Supports Hot-Swapping and Cold Sparing
- Configurable I/O Support 3.3V/5.0V PCI, LVTTL, TTL and CMOS
- Secure Programming Technology prevents reverse engineering
- SX-A Pin compatibility for prototyping with commercial devices
- QML Certified Devices

<table>
<thead>
<tr>
<th></th>
<th>SX32S</th>
<th>SX72S</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Gates</td>
<td>48k</td>
<td>108k</td>
</tr>
<tr>
<td>Logic Modules</td>
<td>2880</td>
<td>6048</td>
</tr>
<tr>
<td>Registers</td>
<td>1080</td>
<td>2016</td>
</tr>
<tr>
<td>Max User I/O</td>
<td>224</td>
<td>205</td>
</tr>
<tr>
<td>Packages</td>
<td>CQ208</td>
<td>CQ256</td>
</tr>
<tr>
<td></td>
<td>CQ208</td>
<td>CQ256</td>
</tr>
</tbody>
</table>
RTSX-S SEU Leadership

Practical SEU Immunity

Cross Section

SER RAM FPGA

RTSX32S

LET (MeV-cm²/mg)

E-12 E-11 E-10 E-09 E-08 E-07 E-06
Benefits of flash FPGA technology

- Lowest power in its class
- In-system programmable
- Non-volatile
- Single-chip
- Secure
- Live at power-up
- Fine grained arch. for ASIC flow
- Flash to ASIC/Conversion Program

<table>
<thead>
<tr>
<th>Product</th>
<th>Process</th>
<th>K Gates</th>
<th>Max I/O</th>
<th>Leading features</th>
</tr>
</thead>
<tbody>
<tr>
<td>ProASIC</td>
<td>0.25um</td>
<td>475</td>
<td>440</td>
<td>ASIC alternative, single-chip</td>
</tr>
<tr>
<td>ProASICPLUS</td>
<td>0.22um</td>
<td>1000</td>
<td>712</td>
<td>ASIC design flow, security lock</td>
</tr>
</tbody>
</table>
### ProASIC A500K Family

#### Features
- Reprogrammable
- Live at power-up
- Single-Chip
- Low Power

#### ASIC Alternative
- Fine Grain Architecture
- Register rich
- ASIC Design Flow

#### FIFO Control Logic

#### Design Security

<table>
<thead>
<tr>
<th>Features</th>
<th>K050</th>
<th>K130</th>
<th>K180</th>
<th>K270</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Gates</td>
<td>100k</td>
<td>290k</td>
<td>370k</td>
<td>475k</td>
</tr>
<tr>
<td>Max Registers</td>
<td>5.4k</td>
<td>12.8k</td>
<td>18.4k</td>
<td>26.9k</td>
</tr>
<tr>
<td>RAM Bits</td>
<td>45k</td>
<td>54k</td>
<td>63k</td>
<td></td>
</tr>
<tr>
<td>RAM Blocks</td>
<td>6</td>
<td>20</td>
<td>24</td>
<td>28</td>
</tr>
<tr>
<td>Max User I/O</td>
<td>204</td>
<td>306</td>
<td>362</td>
<td>440</td>
</tr>
<tr>
<td>Packages</td>
<td>PQ208</td>
<td>PQ208</td>
<td>PQ208</td>
<td>BG456</td>
</tr>
<tr>
<td></td>
<td>BG272</td>
<td>BG272</td>
<td>BG272</td>
<td>BG456</td>
</tr>
<tr>
<td></td>
<td>FG144</td>
<td>BG456</td>
<td>FG256</td>
<td>FG672</td>
</tr>
</tbody>
</table>
ProASICPLUS Overview

Enhancements from the ProASIC architecture

- 0.22m 4LM Flash-Based CMOS FPGA
- Increased programmable logic up to 56K registers
- Larger amount of configurable SRAM up to 198kbits
- Double the high-performance routing resources
- Two PLLs (1.5 to 240 MHz) with multiply, divide and delay options
- Two high speed LVPECL differential pairs (Clock or Data inputs)
- Higher performance I/Os with 50 MHz PCI
- Improved In-system programming
# ProASICPlus Family

<table>
<thead>
<tr>
<th></th>
<th>APA150</th>
<th>APA300</th>
<th>APA450</th>
<th>APA600</th>
<th>APA750</th>
<th>APA1000</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>System Gates</strong></td>
<td>150,000</td>
<td>300,000</td>
<td>450,000</td>
<td>600,000</td>
<td>750,000</td>
<td>1,000,000</td>
</tr>
<tr>
<td><strong>Max Registers</strong></td>
<td>6,144</td>
<td>8,192</td>
<td>12,288</td>
<td>21,504</td>
<td>32,678</td>
<td>56, 320</td>
</tr>
<tr>
<td><strong>Embedded RAM Bits</strong></td>
<td>36k</td>
<td>72k</td>
<td>108k</td>
<td>126k</td>
<td>144k</td>
<td>198k</td>
</tr>
<tr>
<td><strong>Max User I/O</strong></td>
<td>232</td>
<td>280</td>
<td>332</td>
<td>472</td>
<td>232</td>
<td>712</td>
</tr>
<tr>
<td><strong>Packages</strong></td>
<td>PQ 208</td>
<td>PQ 208</td>
<td>PQ 208</td>
<td>PQ 208</td>
<td>PQ 208</td>
<td>PQ 208</td>
</tr>
<tr>
<td></td>
<td>BG 456</td>
<td>BG 456</td>
<td>BG 456</td>
<td>BG 456</td>
<td>BG 456</td>
<td>BG 456</td>
</tr>
<tr>
<td></td>
<td>FG 144</td>
<td>FG 144</td>
<td>FG 144</td>
<td>FG 256</td>
<td>FG 676</td>
<td>FG 896</td>
</tr>
<tr>
<td></td>
<td>FG 256</td>
<td>FG 256</td>
<td>FG 256</td>
<td>FG 256</td>
<td>FG 676</td>
<td>FG 1152</td>
</tr>
</tbody>
</table>
ProASIC/ProASICPLUS In-System Programming

- ProASICPLUS enhanced ISP features
  - Micro-processor interface
  - Chip remains powered-up during programming
- ISP Demo Board available in 1Q02
  - Program daisy chained devices
  - Application note & user guide provided
- App note includes
  - Board schematics
  - Bill of materials
  - Software requirements for ISP interface
ProASIC\textsuperscript{PLUS} In-System Programmer

- Small form factor - 24 in\textsuperscript{3}
- Low cost
- Hardware features
  - Small 26-pin header
  - 20” ribbon cable
  - ECP parallel port
- Software features
  - Win 95/98/NT/00 O/S
  - STAPL support
  - Daisy chain capability
  - Log file generation
Flash to ASIC Conversion Program

- Certified ASIC Partner - Faraday
- ASICs fabricated by UMC
- Facilitated by ProASIC fine grain architecture
- Minimizes conversion risks
- Supports all ProASIC parts
- Supports PQ and BGA packages
- Supports Commercial and Industrial temperatures
- Low risk and cost effective
Actel Product Spectrum

Markets
- Full Featured FPGA
  - Express
- Economy FPGA
  - ProASIC PLUS
  - ProASIC
  - SX-A
- CPLD Equivalent
  - eX

Density
- 3,000
- 10,000
- 100,000
- 1M
- 2M
Agenda

- Introduction
- Product Overview
- Strategic Direction
Opportunity for Embedded FPGA

Worldwide UPL Shipments

- CPLD & FPGA market position fund EPGA opportunity
- Actel SoC/EPGA strategies: BridgeFPGA™ & VariCore™
Increasing Bandwidth in the Network

Each generation brings
- More speed
- New standards
- Interoperability challenges
Actel Focuses on Interoperability

- General purpose FPGA combined with soft-IP
- BridgeFPGA™, configurable bridges for emerging standards
- VariCore™ embedded FPGA cores
BridgeFPGA™ Concept

- High-speed I/O
  - Up to 3.125Gbps
  - Multiple standards
- ASIC for performance, cost & power
- FPGA for flexibility
  - Control & memory interface
  - Protocol translation
- Fast-turn methodology
  - Supports emerging standards

General Purpose FPGA CORE

Configurable I/O (LVDS, ...)
Configurable Protocol Controllers

Control System (uP, PCI, PCI-X, ...)

Memory System (ZBT, DDR, QDR)

High-Speed Data

General Purpose I/O
VariCore EPGA™ Family

- Licensable FPGA core
  - 0.18um SRAM FPGA technology
  - Block sizes: 5K - 40K ASIC gates
  - 2K ASIC gates/mm²
  - 0.13um in development

- UMC, CSM & TSMC processes

- Product Support
  - Complete development environment
  - Debug/probing capability
  - Developers kit with eval board
  - Flow support for most popular SoC EDA tools
  - Embedded configuration, power control, BIST, & JTAG interfaces
Summary

- Actel’s antifuse technology delivers
  - High performance
  - Low power
  - Secure
  - Live at power-up

- Actel’s Flash technology delivers
  - Nonvolatility and reprogrammability
  - Low power
  - Secure
  - Live at power-up

- Strategic developments
  - Licensable VariCore™ FPGA cores to enable PSOC
  - BridgeFPGA™ addresses interoperability needs
Space.......Where failure is not an option!