Books

A. Crouch.
Design for Test for Digital ICs and Embedded Core Systems

M. Abramovici, M. Breuer, A. Friedman.
Digital System Testing and Testable Design

A.J. van der Goor.
Testing Semiconductor Memories: Theory and Practice

K.P. Parker.
The Boundary-Scan Handbook

J. Rajski, J. Tyszer.
Arithmetic Built-In Self-Test For Embedded Systems

Magazines and Journals

IEEE Design and Test of Computers
IEEE Transactions on CAD
IEEE Transactions on Computers
Journal of Electronic Testing (JETTA)
Conferences and Workshops

Conferences/Tutorials

• International Test Conference (ITC)
• Design Automation Conference (DAC)
• European Design and Test Conference
• VLSI Test Symposium (VTS)

Workshops

• Testing Embedded Core-based Systems
• Memory Technology, Design, and Testing
• DFT and BIST Workshops
• Test Synthesis Workshop

Additional Literature

International Technology Roadmap for Semiconductors
ASIC vendors reference manuals and web pages
EDA vendor reference manuals and web pages
Patent descriptions and US Patent and Trademark Office web site

There are many patents in DFT!
References


IEEE P1500 SECT. P1500 General Information.

http://www.manta.ieee.org/groups/1500/#GeneralInfo


M. Lousberg et.al. P1500’ s Core Test Language.

http://www.manta.ieee.org/groups/1500


E. Marinissen, Y. Zorian, R. Kapur, T. Taylor, L. Whetsel. Towards


http://www.manta.ieee.org/groups/1500


VSI Alliance. VSI Alliance Architecture Document. 

http://www.vsi.org/library

K.D. Wagner. Robust scan-based logic test in VDSM technologies.