Programmable Logic Devices and Architectures

R. Roosta
What We Will Cover

• programmable logic types
• Device architectures
• Device performance
• Packaging
• Reliability
• Radiation considerations
• Lessons learned
Applications

• Existing SSI/MSI Integration
• Obsolete/"Non-Space-Qualified" Component Replacement
• Bus Controllers/Interfaces
• Memory Controller/Scrubber
• High-Performance DSP
• Processors
• Systems on a Chip (SOC)
• Other Digital Circuits
SSI/MSI Logic Integration
Non-Space Qual Microcontroller
Complex System-on-Chip

- CAN Network >100Mbps
- 170Mbyte Microdrive
- TX 1M*64 SRAM
- CAN BUS LVDS
- RX0, RX1, RX2
- LEON Sparc V8
- AMBA AHB CAN Interface
- AMBA AHB HDLC TX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB HDLC RX Controller
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- AMBA AHB FIFO
- LEON Sparc V8
- CORDIC Coprocessor
- CF+ I/F True IDE
- ROM LUT Bootstrap
- EDAC DECDED
- 1M*64 SRAM
- UART
- PIO
- Linear Regulator
- +2.5V +3.3V
- System Bus

Clocks: CLK, CLK, CLK, CLK, CLK

- POR
- SSSTL Core
- ESA Core

- CAN
- BUS LVDS
- FIFO
Programmable Elements Overview

- **Antifuse** (Actel)
  - ONO and Metal-to-Metal (M2M)
  - Construction
  - Resistance
- **SRAM Based** (Xilinx)
  - Structure
  - Quantity
- EEPROM/Flash
- Ferro-electric Memory
- Summary of Properties
Antifuse Technology

ONO Antifuse (Actel)

Poly/ONO/N++
Heavy As doped Poly/N++
Thickness controlled by CVD nitride
Programs ~ 18V
Typical Toxono ~ 85 Å
Hardened Toxono ~ 95 Å
R = 200 - 500 ohms

Metal-to-Metal Antifuse (Actel, UTMC, Quicklogic)

‘Pancake’ Stack Between Metal Layers
Used in 3.3V Operation in Sea Of Gates FPGA
Other devices (as shown later)
Program at ~ 10V
Typical thickness ~ 500 - 1000 Å
R = 20 - 100 ohms
Antifuse Cross-Sections

ONO
(Act 1)

Amorphous Silicon
(Vialink)
M2M Antifuse in Multi-layer Metal Process

SX, SX-A, and SX-S

Vialink

M2M = Metal-to-metal
Programmed Antifuse Resistance Distributions

The resistance of programmed antifuses is stable with temperature, varying less than 15 percent per 100°C.
SRAM Switch Technology

Configuration Memory Cell

Read or Write
Data

Routing Connections
Xilinx 4000XL Series FPGAs

- Gate Count (k Gates)
- Bit Count
- Registers
- Max User Ram
- Configuration Bits
# Summary of Current Technology

<table>
<thead>
<tr>
<th>Type</th>
<th>Re-programmable</th>
<th>Volatile</th>
<th>Technology</th>
<th>Radiation Hardness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fuse</td>
<td>No</td>
<td>No</td>
<td>Bipolar</td>
<td>Hard</td>
</tr>
<tr>
<td>EPROM</td>
<td>Yes</td>
<td>No</td>
<td>UVC莫斯</td>
<td>Moderate</td>
</tr>
<tr>
<td>EEPROM</td>
<td>YES, ICP</td>
<td>No</td>
<td>EECMOS</td>
<td>Moderate</td>
</tr>
<tr>
<td>SRAM</td>
<td>YES, ICP</td>
<td>Yes</td>
<td>CMOS</td>
<td>Soft</td>
</tr>
<tr>
<td>Antifuse</td>
<td>No</td>
<td>No</td>
<td>CMOS+</td>
<td>Hard</td>
</tr>
</tbody>
</table>
| FRAM      | Yes, ICP        | No       | Perovskite     | Hard\(^1\)         | Ferroelectric Crystal
FPGA Architecture

- Assembly of Fundamental Blocks
  - Hierarchical
  - Integration of Different Building Blocks
    - Logic (Combinational and Sequential)
    - Dedicated Arithmetic Logic
    - Clocks
    - Input/Output
    - Delay Locked Loop (DLL)
    - RAM

- Routing (Interconnections)
  - Channeled Architecture
  - Sea-of-Module Architecture
Channel Architecture
Channeled Routing Structure

Programmed Antifuse
Horizontal Track

Unprogrammed Antifuse

Modules

Horizontal Control

Vertical Track
Act 3 Architecture Detail

An Array with \( n \) rows and \( m \) columns

<table>
<thead>
<tr>
<th>Rows</th>
<th>Channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>( n+2 )</td>
<td>( n+1 )</td>
</tr>
<tr>
<td>( n+1 )</td>
<td>( n )</td>
</tr>
<tr>
<td>( n )</td>
<td>( n-1 )</td>
</tr>
<tr>
<td>( n-1 )</td>
<td>( 2 )</td>
</tr>
<tr>
<td>( 2 )</td>
<td>( 1 )</td>
</tr>
<tr>
<td>( 1 )</td>
<td>( 0 )</td>
</tr>
</tbody>
</table>

- Left I/Os
- Right I/Os
- Bottom I/Os
- Top I/Os
Sea-of-Modules Structure

• Some programmable elements require silicon resources
  – SRAM flip-flops
  – ONO antifuse

• Metal-to-metal antifuses are built above the logic
  – No routing channels
  – Higher density
  – Faster
UT4090 Architecture

RAM Blocks

Logic Array

RAM Blocks
Virtex Architecture Overview

IOB = I/O Block
DLL = Delay-locked loop
BRAM = Block RAM
    (4,096 bits ea.)
CLB = Configurable Logic Block
Two Slice Virtex CLB
Logic Modules

• **Actel (Act 1,2,3, SX)**
  – Basics
  – Flip-flop Construction

• **UTMC/Quicklogic (i.e., UT4090)**
  – RAM blocks

• **Xilinx (i.e., CQR40xxXL, Virtex,VirtexII)**
  – LUTs/ BlockRAM
  – Carry Logic/Chain

• **Mission Research Corp. (MRC) - Orion**

• **Atmel - AT6010**
Act 2 Logic Module: C-Mod

8-Input Combinational function

766 possible combinational macros

Act 2 Flip-flop Implementation

Feedback goes through antifuses (R) and routing segments (C)

Hard-wired Flip-flop

Routed or “C-C Flip-flop”
SX-S R-Cell Implementation
UT4090 Logic Module

- Antifuse Configuration Memory
- Mux-based
- Multiple Outputs
- Wide logic functions
UT4090 RAM Module

- Dual-port
- 1152 bits per cell
- Four configurations
  - 64 X 18
  - 128 X 9
  - 256 X 4
  - 512 X 2
XC4000 Series CLB
Simplified CLB - Carry Logic Not Shown

RAM LUTs for Logic or small SRAM

Two Flip-flops
XQR4000XL Carry Path

Placement is important for performance.
Carry Logic Operation

Effective Carry Logic for a Typical Addition - XQR4000XL
MRC Orion Logic Module
AT60xx Logic Module
Memory Architecture

• Radiation-hardened PROM
• Configuration Memory
• EEPROM
Rad-Hard PROM Architecture

No latches in this architecture
Configuration PROM Example

Figure 1: Simplified Block Diagram (does not show programming circuit)
W28C64 EEPROM
Simplified Block Diagram

Row Address Latches

Column Address Latches

Row Address Decoder

Column Address Decoder

E\(^2\) Memory Array

64 Byte Page Buffer

Edge Detect & Latches

Latch Enable

Control Latch

Control Logic

Timer

I/O Buffer/Data Polling

A\(_{6-12}\)

A\(_{0-5}\)

CE*

WE*

OE*

CLK

VW

I/O\(_{0-7}\)

PE

RSTB
Input/Output Modules
A Brief Overview

• Basic Input/Output (I/O) Module
• Some Features
  – Slew Rate Control
  – Different I/O Standards
  – Input Delays
  – Banks
• Deterministic Powerup
• Cold Sparing
Act 1

- Many families have slew rate control to limit signal reflections and ground bounce.
- Different families drive their outputs to different levels.
## Different I/O Standards

**Virtex 2.5V Example**

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>Input Ref Voltage ($V_{\text{REF}}$)</th>
<th>Output Source Voltage ($V_{\text{CCO}}$)</th>
<th>Board Termination Voltage ($V_{\text{TT}}$)</th>
<th>5V Tolerant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVTTL 2–24 mA</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
<td>Yes</td>
</tr>
<tr>
<td>LVCMOS2</td>
<td>N/A</td>
<td>2.5</td>
<td>N/A</td>
<td>Yes</td>
</tr>
<tr>
<td>PCI, 5 V</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
<td>Yes</td>
</tr>
<tr>
<td>PCI, 3.3 V</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
<td>No</td>
</tr>
<tr>
<td>GTL</td>
<td>0.8</td>
<td>N/A</td>
<td>1.2</td>
<td>No</td>
</tr>
<tr>
<td>GTL+</td>
<td>1.0</td>
<td>N/A</td>
<td>1.5</td>
<td>No</td>
</tr>
<tr>
<td>HSTL Class I</td>
<td>0.75</td>
<td>1.5</td>
<td>0.75</td>
<td>No</td>
</tr>
<tr>
<td>HSTL Class III</td>
<td>0.9</td>
<td>1.5</td>
<td>1.5</td>
<td>No</td>
</tr>
<tr>
<td>HSTL Class IV</td>
<td>0.9</td>
<td>1.5</td>
<td>1.5</td>
<td>No</td>
</tr>
<tr>
<td>SSTL3 Class I &amp;II</td>
<td>1.5</td>
<td>3.3</td>
<td>1.5</td>
<td>No</td>
</tr>
<tr>
<td>SSTL2 Class I &amp; II</td>
<td>1.25</td>
<td>2.5</td>
<td>1.25</td>
<td>No</td>
</tr>
<tr>
<td>CTT</td>
<td>1.5</td>
<td>3.3</td>
<td>1.5</td>
<td>No</td>
</tr>
<tr>
<td>AGP</td>
<td>1.32</td>
<td>3.3</td>
<td>N/A</td>
<td>No</td>
</tr>
</tbody>
</table>
Virtex 2.5V
Deterministic Power-up
SX-S Example

- Pull-ups /downs are selectable on an individual I/O basis
- Pull-up follows $V_{CCI}$
- Pull-downs and pull-ups are disabled 50 ns after $V_{CCA}$ reaches 2.5V and therefore do not draw current during regular operation.
- Once $V_{CCA}$ is powered-up, 50ns is required for a valid signal to propagate to the outputs before the pull-ups /downs are disabled
Cold Sparing - SX-S

- **Powered-up Board**
  - 3.3/5 Volts
  - $V_{CCI}$
  - RTSX-S
  - GND

- **Powered-down Board**
  - 0 Volts
  - $V_{CCI}$
  - RTSX-S
  - GND

- **Active Bus or Backplane**
  - I/O w/ ”Hot-Swap” Enabled does not sink current
Packaging and Mechanical Aspects

- Package Types
  - Dual In-line Package (DIPs)
  - Flatpacks
  - Pin Grid Arrays (PGAs)
  - Ceramic Quad Flat Packs (CQFP)
  - Plastic Quad Flat Pack (PQFP)

- Plastic Package Qualification
- Lead/Ball Pitch
- Mass Characteristics
- Shielding
Flat Pack
Northrop-Grumman 256k EEPROM
Shielded Packages - Rad-Pak™

- This package, with tie bar, 24 grams
- Shielding thickness may vary between lots
- Shield is 10-90/copper-tungsten
- Density of shield is ~ 18 g/cm³ (need to verify)
- EEPROMs and other devices also packaged similarly
Spot Shielding Qualification Board - Maximum Thickness
PGA Packages (cont'd)
PQFP Package
## Nominal Lead/Ball Pitch

<table>
<thead>
<tr>
<th>Code</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CQ84</td>
<td>0.025&quot;</td>
</tr>
<tr>
<td>CQ132</td>
<td>0.025&quot;</td>
</tr>
<tr>
<td>CQ172</td>
<td>0.025&quot;</td>
</tr>
<tr>
<td>CQ196</td>
<td>0.025&quot;</td>
</tr>
<tr>
<td>CQ208</td>
<td>0.50 mm</td>
</tr>
<tr>
<td>PQ208</td>
<td>0.50 mm</td>
</tr>
<tr>
<td>CQ256</td>
<td>0.05 mm</td>
</tr>
<tr>
<td>CG560</td>
<td>1.27 mm</td>
</tr>
</tbody>
</table>

Note: Pin spacing for PGAs is typically 0.1"
Mass Characteristics
Approximate values (in grams)

<table>
<thead>
<tr>
<th>Part</th>
<th>Mass (g)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CQ84</td>
<td>2.2</td>
</tr>
<tr>
<td>CQ132</td>
<td>5.8</td>
</tr>
<tr>
<td>CQ172</td>
<td>8.8</td>
</tr>
<tr>
<td>CQ196</td>
<td>11.1</td>
</tr>
<tr>
<td>CQ208</td>
<td>8.8</td>
</tr>
<tr>
<td>CQ208(^1)</td>
<td>18.5</td>
</tr>
<tr>
<td>PQ208</td>
<td>5.2</td>
</tr>
<tr>
<td>CB228</td>
<td>17.6</td>
</tr>
<tr>
<td>CQ256</td>
<td>13.0</td>
</tr>
<tr>
<td>CQ256(^\d)</td>
<td>20.2</td>
</tr>
<tr>
<td>PG84</td>
<td>8.0</td>
</tr>
<tr>
<td>PG133</td>
<td>11.0</td>
</tr>
<tr>
<td>PG176</td>
<td>19.0</td>
</tr>
<tr>
<td>PG207</td>
<td>24.5</td>
</tr>
<tr>
<td>PG207(^\d)</td>
<td>24.5</td>
</tr>
<tr>
<td>PG257</td>
<td>27.3</td>
</tr>
<tr>
<td>BG560</td>
<td>11.5</td>
</tr>
<tr>
<td>CG560</td>
<td>11.5</td>
</tr>
</tbody>
</table>

\(^1\)With heat sink. Over the years, there has been a lot of variation as to which parts have heat sinks. Check each package.
Reliability

- Introduction to Reliability
- Historical Perspective
- Current Devices
- Trends
The Bathtub Curve

Failure rate, \( \lambda \)

- Infant Mortality
- Useful life
- Wear out

\( \lambda \) Constant

Time
Introduction to Reliability

• **Failure in time (FIT)**
  
  Failures per $10^9$ hours

  ($\sim 10^4$ hours/year)

• **Acceleration Factors**

  – Temperature

  – Voltage
Most failure mechanisms can be modeled using the Arrhenius equation.

\[ ttf = C \cdot e^{\frac{E_A}{kT}} \]

- \( ttf \) - time to failure (hours)
- \( C \) - constant (hours)
- \( E_A \) - activation energy (eV)
- \( k \) - Boltzmann's constant \((8.616 \times 10^{-5} \text{eV/°K})\)
- \( T \) - temperature (°K)
### Integrated Circuit Reliability

**Historical Perspective**

<table>
<thead>
<tr>
<th>Application</th>
<th>Reliability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apollo Guidance Computer</td>
<td>&lt; 10 FITs</td>
</tr>
<tr>
<td>Commercial</td>
<td>(1971) 500 Hours</td>
</tr>
<tr>
<td>Military</td>
<td>(1971) 2,000 Hours</td>
</tr>
<tr>
<td>High Reliability</td>
<td>(1971) 10,000 Hours</td>
</tr>
<tr>
<td>SSI/MSI/PROM 38510</td>
<td>(1976) 44-344 FITs</td>
</tr>
<tr>
<td>MSI/LSI CICD Hi-Rel</td>
<td>(1987) 43 FITs</td>
</tr>
</tbody>
</table>
## Actel FPGAs

<table>
<thead>
<tr>
<th>Technology (µm)</th>
<th>FITS</th>
<th># Failures</th>
<th>Device-Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0/1.2</td>
<td>33</td>
<td>2</td>
<td>9.4 x 10^7</td>
</tr>
<tr>
<td>1.0</td>
<td>9.0</td>
<td>6</td>
<td>6.1 x 10^8</td>
</tr>
<tr>
<td>0.8</td>
<td>10.9</td>
<td>1</td>
<td>1.9 x 10^8</td>
</tr>
<tr>
<td>0.6</td>
<td>4.9</td>
<td>0</td>
<td>1.9 x 10^8</td>
</tr>
<tr>
<td>0.45</td>
<td>12.6</td>
<td>0</td>
<td>7.3 x 10^7</td>
</tr>
<tr>
<td>0.35</td>
<td>19.3</td>
<td>0</td>
<td>4.8 x 10^7</td>
</tr>
<tr>
<td>RTSX 0.6</td>
<td>33.7</td>
<td>0</td>
<td>2.7 x 10^7</td>
</tr>
<tr>
<td>0.25</td>
<td>88.9</td>
<td>0</td>
<td>1.0 x 10^7</td>
</tr>
<tr>
<td>0.22</td>
<td>78.6</td>
<td>0</td>
<td>1.2 x 10^7</td>
</tr>
</tbody>
</table>
Xilinx FPGAs

• **XC40xxXL**
  - Static:  9 FIT, 60% UCL
  - Dynamic: 29 FIT, 60% UCL

• **XCVxxx(Virtex)**
  - Static:  34 FIT, 60% UCL
  - Dynamic: 443 FIT, 60% UCL
UTMC and Quicklogic

• FPGA
  – < 10 FITS (planned)
  – Quicklogic reports 12 FIT, 60% UCL

• UT22VP10
  UTER Technology, 0 failures, 0.3 [double check]

• Antifuse PROM
  – 64K: 19 FIT, 60% UCL
  – 256K: 76 FIT, 60% UCL
Actel FIT Rate Trends

Table 8-1  Fit Rates

<table>
<thead>
<tr>
<th>Time Period</th>
<th>Q2,96</th>
<th>Q1,97</th>
<th>Q2,97</th>
<th>Q3/Q4, 97</th>
<th>Q1,98</th>
<th>Q2,98</th>
<th>Q3,98</th>
<th>Q4,98</th>
<th>Q1,99</th>
<th>Q2,99</th>
<th>Q3,99</th>
<th>Q4,99</th>
<th>Q1, 00</th>
</tr>
</thead>
<tbody>
<tr>
<td>1μ (FITS)</td>
<td>13.87</td>
<td>13.37</td>
<td>13.29</td>
<td>12.9</td>
<td>10.9</td>
<td>10.3</td>
<td>10.3</td>
<td>10.3</td>
<td>10.3</td>
<td>10.3</td>
<td>10.3</td>
<td>9.43</td>
<td>9.43</td>
</tr>
<tr>
<td>0.8μ (FITS)</td>
<td>20</td>
<td>19</td>
<td>19</td>
<td>18.5</td>
<td>16.6</td>
<td>16.6</td>
<td>15.5</td>
<td>15.5</td>
<td>15.5</td>
<td>15.5</td>
<td>15.5</td>
<td>15.5</td>
<td>14.77</td>
</tr>
<tr>
<td>0.6μ (FITS)</td>
<td>18</td>
<td>12.11</td>
<td>10.87</td>
<td>5.75</td>
<td>5.68</td>
<td>5.36</td>
<td>5.36</td>
<td>5.36</td>
<td>5.36</td>
<td>5.36</td>
<td>5.36</td>
<td>5.01</td>
<td>4.85</td>
</tr>
<tr>
<td>0.45μ (FITS)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>90.4</td>
<td>30</td>
<td>25</td>
<td>25</td>
<td>23.53</td>
<td>23.53</td>
</tr>
<tr>
<td>0.35μ (FITS)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>96</td>
<td>35</td>
<td>35</td>
<td>29.2</td>
<td>29.2</td>
</tr>
<tr>
<td>RTSX 0.6μ (FITS)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>145</td>
<td>145</td>
<td>74.6</td>
</tr>
<tr>
<td>0.25μ (FITS)</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>145</td>
<td>145</td>
</tr>
</tbody>
</table>

Figure 8-1  FIT Rates
Thermal

- Thermal Analysis Basics
- Summary of Package Characteristics
- Package Considerations
  - Cavity Up/Down
  - Heat Sinks
Thermal Performance

• Package modeled as a resistance

• Junction temperature the critical parameter
  – Often derated to $\sim 100 \, ^{\circ}\text{C}$

• $t_J = P \cdot \theta_{J-C}$

  $t_J$ = Junction temperature in $^{\circ}\text{C}$
  $P$ = Power in watts
  $\theta_{J-C}$ = thermal resistance, junction to case, in $^{\circ}\text{C}$/watt
# Thermal Performance - Devices

$\theta_{J-C}$ for Flight Devices in °C/watt

<table>
<thead>
<tr>
<th>Ceramic Pin Grid Array</th>
<th>Ceramic Quad Flat Pack</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG84  6.0</td>
<td>CQ84  7.8</td>
</tr>
<tr>
<td>PG133 4.8</td>
<td>CQ132 7.2</td>
</tr>
<tr>
<td>PG176 4.6</td>
<td>CQ172 6.8</td>
</tr>
<tr>
<td>PG207 3.5(^1)</td>
<td>CQ196 6.4</td>
</tr>
<tr>
<td>PG257 2.8(^1)</td>
<td>CQ208 6.3</td>
</tr>
<tr>
<td></td>
<td>CQ256 6.2</td>
</tr>
<tr>
<td></td>
<td><strong>Other</strong></td>
</tr>
<tr>
<td></td>
<td>PQ208 8.0/3.8(^2)</td>
</tr>
<tr>
<td></td>
<td>PQ240 2.8(^4)</td>
</tr>
<tr>
<td></td>
<td>HQ240 1.5(^4)</td>
</tr>
<tr>
<td></td>
<td>CG560 0.8(^3)</td>
</tr>
</tbody>
</table>

**Notes:**

\(^1\)These packages are cavity down.

\(^2\)With embedded heat spreader

\(^3\)Estimated

\(^4\)Typical
Die Up or Down?

A. Die Up/Heatsink Down

B. Die Down/Heatsink Up
Speed/Performance

- Basic Delay Model and Components
- Sample Delays
  - Examples from different families
- Hard-wired Structures
  - Routing
  - Arithmetic Logic
Antifuse Delay Model

\[
\tau = \text{Resistance} \times \text{Capacitance}
\]
Unprogrammed Antifuse Capacitance

Note: These numbers are approximate and work on better numbers is in progress. UTMC, for PAL and PROM, has about 8 to 10 fF.
Propagation Delay of Actel Flight FPGAs

- t\textsubscript{PD} w/ Direct Connect Routing
- t\textsubscript{PD} w/ Fast Connect Routing
- t\textsubscript{PD}, fanout=1, regular routing
- t\textsubscript{PD}, fanout=4, regular routing

**Notes:**
Values from Data Sheets
Worst-case values listed
Use timing extraction to obtain values for real circuits
# Hardwired Structures

## Actel Routing

<table>
<thead>
<tr>
<th>Model</th>
<th>Direct Connect (ns)</th>
<th>Fast Connect (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT54SX-1</td>
<td>0.2</td>
<td>1.1</td>
</tr>
<tr>
<td>RT54SXS-1</td>
<td>0.1</td>
<td>0.4</td>
</tr>
</tbody>
</table>

## Virtex Carry Chain

\[ T_{BYP} \ (C_{IN} \ to \ C_{OUT}) \quad 200 \ \text{ps, max} \]
Power Consumption

• Power Basics
• Quiescent (Static) Current
• Dynamic Current
  – Per logic module
  – Clock tree
Power - Basics

- Power = Voltage * current = V i
- Voltage is constant
- Current = Static + Dynamic

- Static current: leakage, pull-up resistors, DC loads

- Dynamic Power = kv²f
  - k: constant often referred to as $C_{EQ}$
  - f: frequency
Relative Power as a Function of Supply Voltage
## Device (Array) Quiescent Current

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Voltage (V)</th>
<th>Typical I&lt;sub&gt;CC&lt;/sub&gt; (mA)</th>
<th>Spec Level I&lt;sub&gt;CCMAX&lt;/sub&gt; (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A500K050</td>
<td>2.5</td>
<td>&lt; 1</td>
<td>10&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Orion-4K</td>
<td>5.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RT1020</td>
<td>5.0</td>
<td>&lt; 1</td>
<td>20</td>
</tr>
<tr>
<td>RT1280A</td>
<td>5.0</td>
<td>&lt; 1</td>
<td>20</td>
</tr>
<tr>
<td>RT14100A</td>
<td>5.0</td>
<td>&lt; 1</td>
<td>20</td>
</tr>
<tr>
<td>RT54SX32</td>
<td>3.3</td>
<td>&lt; 1</td>
<td>25</td>
</tr>
<tr>
<td>RT54SX32S</td>
<td>2.5</td>
<td>&lt; 1</td>
<td>25</td>
</tr>
<tr>
<td>UT4090</td>
<td>3.3</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>XQR40xxXL</td>
<td>3.3</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>XQV100</td>
<td>2.5</td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>XQV300</td>
<td>2.5</td>
<td></td>
<td>75</td>
</tr>
<tr>
<td>XQV600</td>
<td>2.5</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>XQV1000</td>
<td>2.5</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>AT6010</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>1</sup>No DC Loads  
<sup>2</sup>Commercial Specification

### XQV600 Lot Data (mA)<sup>1</sup>

<table>
<thead>
<tr>
<th>lot #</th>
<th>min</th>
<th>mean</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>1157448</td>
<td>4.72</td>
<td>6.41</td>
<td>8.13</td>
</tr>
<tr>
<td>1152401</td>
<td>6.26</td>
<td>8.37</td>
<td>11.40</td>
</tr>
<tr>
<td>1139803</td>
<td>3.75</td>
<td>5.57</td>
<td>12.85</td>
</tr>
</tbody>
</table>

<sup>1</sup>commercial or industrial worst-case, checking
## PROM Device Current\(^1\)

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Voltage (V)</th>
<th>Standby I(_{cc}) (mA)</th>
<th>Dynamic I(_{cc\text{MAX}}) (mA)</th>
<th>@F (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UT28F64</td>
<td>5.0</td>
<td>0.5</td>
<td>100</td>
<td>28.6(^2)</td>
</tr>
<tr>
<td>UT28F256</td>
<td>5.0</td>
<td>&lt; 2</td>
<td>125</td>
<td>28.6(^2)</td>
</tr>
<tr>
<td>197A8073(^3)</td>
<td>5.0</td>
<td>2.0</td>
<td>200</td>
<td>22.2</td>
</tr>
</tbody>
</table>

\(^1\)Specification levels  
\(^2\)Derates @ 2.5 mA/MHz  
\(^3\)BAE Systems (formerly Lockmart) 32kx8 PROM
## Representative Dynamic Power Numbers

**A1280/A1280XL Power (mW)**

<table>
<thead>
<tr>
<th>F(MHz)</th>
<th>Module</th>
<th>Input</th>
<th>Output</th>
<th>Clock</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>11</td>
<td>13</td>
<td>21</td>
<td>27</td>
<td>72</td>
</tr>
<tr>
<td>2</td>
<td>23</td>
<td>25</td>
<td>42</td>
<td>54</td>
<td>144</td>
</tr>
<tr>
<td>5</td>
<td>57</td>
<td>63</td>
<td>105</td>
<td>136</td>
<td>360</td>
</tr>
<tr>
<td>10</td>
<td>113</td>
<td>125</td>
<td>210</td>
<td>272</td>
<td>720</td>
</tr>
<tr>
<td>20</td>
<td>227</td>
<td>250</td>
<td>419</td>
<td>544</td>
<td>1,440</td>
</tr>
<tr>
<td>30</td>
<td>340</td>
<td>375</td>
<td>629</td>
<td>815</td>
<td>2,159</td>
</tr>
<tr>
<td>40</td>
<td>453</td>
<td>500</td>
<td>839</td>
<td>1,087</td>
<td>2,879</td>
</tr>
</tbody>
</table>
Power Consumption (Logic Module)

Notes:
1. Based on data sheets
2. Nominal voltages used for calculations
3. SX data is "Preliminary"
4. SX-S data is "Advanced"
A Brief Introduction to Radiation and Programmable Devices
Types of Radiation Effects

• Total Dose

• Single Event Effects (SEE)
  – Single Event Upset (SEU)
    • Multiple Bit Upset (MBU)
  – Single Event Latchup (SEL)
  – Single Event Transient (SET)
  – Antifuse and Rupture
  – Loss of Functionality
  – Snap back

• Protons

• Miscellaneous
Total Dose
Recombination, Transport, and Trapping of Carries

Carrier transport mechanism

(a) $t = 0^-$ (PRE-IRRADIATION)

(b) $t = 0$ (IONIZING BURST)

(c) $t = 0^+$ (AFTER INITIAL RECOMBINATION)

(d) $t = 0^+$ (AFTER ELECTRON TRANSPORT)

(e) $t = t_1$ (HOLE TRANSPORT IN PROGRESS)

(f) $t = t_2$ (AFTER HOLE TRANSPORT)

FIGURE 5. Illustration of recombination, transport, and trapping of carriers in SiO$_2$ films.
Typical TID Run

A1425A/MEC TID TEST
D/C 9819 - UCJ014X
6 kRads (Si) / Day
NASA/GSFC
August 14, 1998

![Graph showing Typical TID Run with multiple S/N LAN20x traces]
TID Run - Runaway

QL3025-2 ESPQ208R TID TEST
D/C 9913CA
18.6 krad (Si) / Day
NASA/GSFC
April 14, 1999

Notes:
1. DUT in Pb-Al box per 1019.5
2. Experimental Device

Power Supply Limit = 800 mA
Submicron FPGA TID Tolerance
0.35 µm to 0.6 µm

- RT54SX16 Proto, 0.6 µm, 3.3V, MEC
- A54SX16 Proto, 0.35 µm, 3.3V, CSM
- A42MX09, 0.45 µm, 5.0V, CSM
- QL3025, 0.35 µm, 3.3V, TSMC
- XQR4000XL Proto, 0.35 µm, 3.3V, 60 kRads (Si)
- RH54SX16 Proto, 0.6 µm, 3.3V, > 200 kRads (Si)
A54SX32A (Prototype) TID TEST
D/C 9924
P04 Wafer 12 and 20
NASA/GSFC
September 24, 1999

Notes
1. Bias levels are 5.0VDC, 2.5VDC
2. Parts are in Pb/Al box per 1019.5
3. Dose rates between 15.7 and 16.6 rad(Si)/min
Single Event Upset (SEU)
Interaction of a Cosmic Ray and Silicon

From Aerospace
Cross Section versus LET Curve

From Aerospace
Act 2 SEU Flip-Flop Data

Cross Section (cm²/flip-flop)

LET (MeV·cm²/mg)

RH1280
A1280A
XQR4036XL SEU Cross Section

From Lum
Single Event Latchup (SEL)
Latchup Basics

From Harris
BNL 02/98
S/N QL1 Run T2
V_{BIAS} = 5.0V, 3.3V
Titanium @ 0 Deg
LET = 18.8 MeV-cm^2/mg
Antifuse and Rupture
Comparison of Rupture Currents

Technology Development Vehicle

RH1280 S/N 063 Antifuse Rupture

Fluence (ions/cm²)
0 20x10⁶ 40x10⁶ 60x10⁶ 80x10⁶ 100x10⁶

Icc (mA)
30 35 40 45

Vcc = 4.7 VDC; LET = 53; Angle = 0 Degrees

ION Antifuse Rupture

Amorphous Silicon Antifuse Rupture

VCC = 4.7 VDC; LET = 53; Angle = 0 Degrees

ONO Antifuse
ONO Antifuse Breakdown - FA

Mag = 5X

Mag = 20X

Mag = 100X
Protons
**$I_{CC}$ Damage During Proton Testing**

**ASIC and Antifuse FPGA**

QYH530 193 MeV Proton Test  
Flux = $1 \times 10^9$ p/cm$^2$/Sec  
S/N QYHD2 - DITS-2 Lot  
NASA/GSFC  
June 17, 1997

QL3025 Proton Irradiation  
S/N QL6  
June, 1998  
Indiana University Cyclotron  
NASA/GSFC

Note: Device Previously Irradiated for Heavy Ion Testing

Note: Different scales for each run.
RH1280 Proton Upsets

From Lockheed-Martin/Actel

- S module threshold = 30 MeV
- C and Modified S > 148 MeV
Summary
FRAM Memory Functionality Loss During Heavy Ion Test

Strip chart of FM1608 (research fab) current during heavy ion irradiation. The device lost functionality during the test while the current decreased from its normal dynamic levels of approximately 6.3 mA to its quiescent value, near zero. The device recovered functionally and operated normally throughout the latter part of the test. This effect was seen at least three times during the limited testing of this device.